IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

SAMSUNG ELECTRONICS CO. LTD., SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG TELECOMMUNICATIONS AMERICA GENERAL, LLC, SAMSUNG SEMICONDUCTOR, INC., and SAMSUNG AUSTIN SEMICONDUCTOR LLC,	)	
Plaintiffs,	)	C.A. No. 06-720 (***)
v.	)	**REDACTED PUBLIC VERSION**
ON SEMICONDUCTOR CORP. and SEMICONDUCTOR COMPONENTS INDUSTRIES, LLC,	)	
Defendants.	)	

DEFENDANTS' OPENING BRIEF IN SUPPORT OF THEIR MOTION TO DISMISS

MORRIS, NICHOLS, ARSHT & TUNNELL LLP
Karen Jacobs Louden (#2881)
1201 N. Market Street
P.O. Box 1347
Wilmington, DE 19899
(302) 658-9200
klouden@mnat.com
Attorneys for Defendants

OF COUNSEL:
Kenneth R. Adamo
JONES DAY
2727 North Harwood Street
Dallas, TX 75201-1515
(214) 220-3939

T. Gregory Lanier
Behrooz Shariati
JONES DAY
2882 Sand Hill Road, Suite 240
Menlo Park, CA 94025
(650) 739-3939

Original Filing Date: December 27, 2006
Redacted Filing Date: January 8, 2007

TABLE OF CONTENTS

TABLE OF CONTENTS (continued)

TABLE OF CITATIONS

Statutes And Other Authorities

NATURE AND STAGE OF THE PROCEEDINGS

Plaintiff Samsung Electronics Co. Ltd. ("Samsung") and defendants ON Semiconductor Corp. and Semiconductor Components Industries, LLC (collectively, "ON Semiconductor") had been engaged in patent licensing negotiations for over a year, when on November 30, 2006, Samsung abruptly, and without notice to ON Semiconductor, filed this declaratory judgment action, seeking a judicial declaration of non-infringement and invalidity of the three ON Semiconductor patents that were the subject of the negotiations: U.S. Patent No. 5,563,594 (the "'594 patent"), U.S. Patent No. 6,362,644 (the "'644 patent"), and 5,361,001 (the "'001 patent"). (Complaint, D.I. 1). Shortly thereafter, Samsung told ON Semiconductor that it had filed this action and simultaneously presented its first license offer for these patents.

After learning of this declaratory action, ON Semiconductor filed a direct action on Monday, December 4, 2006 in the Eastern District of Texas against Samsung and its affiliates Samsung Electronics America, Inc., Samsung Telecommunications America General, L.L.C., Samsung Semiconductor, Inc., and Samsung Austin Semiconductor, L.L.C. (the "Samsung affiliates"), alleging that they infringe ON Semiconductor's U.S. Patent No. 5,000,827 (the "'827 patent") as well as the '594, '644, and '001 patents. (Ex. A). ON Semiconductor served the Texas complaint on each of the defendants the same day. (Ex. B). Samsung did not serve ON Semiconductor with the Complaint in this action until December 6, 2006. (*See* Summons, D.I. 5 and 6). Samsung then filed an amended complaint on December 21, 2006, adding to this action the Samsung affiliates, a count seeking a judicial declaration of non-infringement and invalidity of the '827 patent, as well as a count alleging infringement of U.S. Patent No. 5,252,177 (the "'177 patent") by ON Semiconductor. (D.I. 8).

ON Semiconductor has filed a motion to dismiss Samsung's declaratory judgment claims for lack of subject matter jurisdiction under Fed. R. Civ. P. 12(b)(1), because there was no case or controversy at the time Samsung originally filed this declaratory judgment action. Because Samsung cannot rely on its amended complaint to create jurisdiction that did not exist at the time of the filing, this motion to dismiss is directed to Samsung's original complaint.[1]

SUMMARY OF ARGUMENT

ON Semiconductor and Samsung had been engaged in long and complex patent negotiations more than a year prior to the filing of this suit. After several face-to-face meetings and telephone conferences, ON Semiconductor extended an offer to Samsung for [redacted]

---

[1] While some motions to dismiss a complaint become moot when a superseding amended complaint is filed, this motion is not moot because Samsung insists it is entitled to the November 30, 2006 filing date of its original complaint. For a Court to have jurisdiction over a declaratory patent infringement action, an "actual controversy *must exist as of the date of the filing* of the declaratory judgment action." Chisum on Patents § 21.02[1][d][iii] (2003 ed) (emphasis added); *see also Spectronics Corp. v. H.B. Fuller Co.*, 940 F.2d 631, 635 (Fed. Cir. 1991) ("Later events may not create [declaratory judgment] jurisdiction where none existed at the time of filing."); *GAF Bldg. Materials Corp. v. Elk Corp. of Dallas*, 90 F.3d 479, 483 (Fed. Cir. 1996) ("[T]he presence or absence of jurisdiction must be determined on the facts existing at the time the complaint under consideration was filed.").

This action cannot have a November 30, 2006 filing date if subject matter jurisdiction is derived from events that occurred *after* November 30, 2006, even if those events are plead in an amended complaint. *Millipore Corp. v. Univ. Patents, Inc.*, 682 F. Supp. 227, 233 (D. Del. 1987) (When an amended declaratory complaint for patent infringement alleges events that occurred after the initial complaint, "the date of filing this amended complaint . . . thereby becomes the controlling date for purposes of determining whether [declaratory plaintiff] had a reasonable apprehension of suit."); *Correspondent Servs. Corp. v. First Equities Corp.*, 338 F.3d 119, 125 (2d Cir. N.Y. 2003) (Courts only relate factual changes in amended complaints back to the date of the original complaint to create jurisdiction "when the underlying facts, if properly pled, *would have supported jurisdiction at the time the action commenced.*") (emphasis added); *see also Metrologic Instruments, Inc. v. PSC, Inc.*, No. 99-4876-JBS, 2004 U.S. Dist. LEXIS 24949, at *53 (D.N.J. Dec. 13, 2004) ("Infringement of one patent is not the same conduct or occurrence as infringement of another patent for the purposes of relation back, unless the claims with respect to the second patent are an integral part of the claims in the first action.") (citations omitted).

[redacted] ON Semiconductor later modified its offer at Samsung's request [redacted] While ON Semiconductor awaited a response to its offer, and in the wake of Samsung's representative stating not once, but twice, that Samsung did not want to litigate, Samsung, apparently maneuvering for advantage in the negotiations, filed a declaratory judgment action on the three patents that had been the subject of the negotiations. Samsung then made its first counteroffer. When asked about the lawsuit, Samsung's representative said that Samsung only wanted "protection" and said that Samsung would not serve the lawsuit because it hoped to settle the matter out of court.

For this Court to have subject matter jurisdiction over Samsung's declaratory judgment action, Samsung must establish that, under the totality of the circumstances, it had an objectively reasonable apprehension that it would be sued based on either an express threat or other actions by ON Semiconductor. Samsung cannot do this. Indeed, all that Samsung alleges in its November 30, 2006 Complaint about ON Semiconductor's actions is that ON Semiconductor accused Samsung of infringing the patents in suit, asked what Samsung believed was too much for a license during negotiations, and said that ON Semiconductor was not going away. Even if true, these facts, at most, signal further negotiation, not an imminent lawsuit. Nor can the fact that ON Semiconductor filed its own suit ***after*** Samsung filed this anticipatory action have created any reasonable apprehension of suit by Samsung during its negotiations with ON Semiconductor.

Even if the Court were to find that an actual controversy existed at the time this suit was filed, this Court should nevertheless exercise its broad discretion to dismiss the declaratory judgment claims. Allowing Samsung's declaratory action to proceed would subvert

both the purposes of the Declaratory Judgment Act and principles of sound judicial administration. The Declaratory Judgment Act was not intended as a means for a party to use a lawsuit as a hammer to extort a more favorable licensing arrangement from a patentee negotiating in good faith. Further, it would be contrary to sound judicial administration to punish ON Semiconductor for seeking a fair value for its intellectual property in license negotiations and to reward Samsung for its improper use of a lawsuit as a negotiating ploy, only because Samsung, in its sole opinion, considered the proposed license fee "exorbitant."

The Court should dismiss the November 30, 2006 declaratory judgment claims for lack of subject matter jurisdiction under Fed. R. Civ. P. 12(b)(1). In the alternative, the Court should exercise its broad discretion not to hear the declaratory actions because allowing them to proceed would undermine the purposes of the Declaratory Judgment Act and contravene sound policy and basic fairness.

STATEMENT OF FACTS

A. The Parties.

ON Semiconductor is a supplier of high-performance power management solutions worldwide. (D.I. 11, Ex. 2). It holds all right, title and interest in the '594, '644, and '001 patents, which are the subject of the November 30, 2006 declaratory judgment complaint. (D.I. 1 ¶ 11; Ex. A-C). Samsung manufactures and markets throughout the world a variety of semiconductor products, including dynamic random access memory ("DRAM") devices. (D.I. 1 ¶ 2).

B. Licensing Negotiations Begin Between ON Semiconductor And Samsung.

For over a year, beginning in September 2005, Samsung and ON Semiconductor were engaged in ongoing negotiations regarding licensing of the '594, '644 and '001 patents. At no time during these lengthy and complex negotiations did ON Semiconductor threaten Samsung with litigation.[2]

Samsung's outside litigation counsel, Mr. Muir, concedes that at the time Samsung filed suit on November 30, "[n]either Mr. Botsch nor any of Defendants' other representatives indicated that Defendants planned to file suit against Samsung within a specific or definite timeframe, nor did they ever indicate that they were considering bringing suit in the Eastern District of Texas."[3] (D.I. 12 ¶16).

The negotiation history confirms Mr. Muir's candid observation and shows that Samsung could not have objectively perceived any threat of imminent litigation, either explicit or implicit. ON Semiconductor initiated negotiations by sending a letter on September 15, 2005 regarding potential licensing of its '594 and '644 patents. (Botsch Dec. ¶ 2, Ex. 1). ON Semiconductor explained that it owns the '594 and '644 patents. (*Id.* at Ex. 1). After noting that "it believe[d]" that Samsung's DRAM devices "infringed the referenced patents," ON

---

2 ON Semiconductor was represented in these negotiations by individuals including Bradley Botsch, ON Semiconductor's Vice President and Chief Intellectual Property Officer, and G. Sonny Cave, ON Semiconductor's Senior Vice President, General Counsel, and Chief Compliance and Ethics Officer. Samsung was represented at various times in these negotiations by individuals including Jay Shim, Vice President, General Manager, and General Patent Counsel at Samsung; Patrick Muir, Samsung's outside licensing counsel; and Jeong Woo Lee, a Samsung employee in Korea.

3 Mr. Muir made this concession in a declaration filed in support of Samsung's pending motion to enjoin ON Semiconductor's direct infringement action in the Eastern District of Texas. *See* "Declaration of Patrick Muir in Support of Plaintiffs' Motion to Enjoin Defendants from Pursuing a Duplicative Texas Action" ("Muir Declaration") (D.I. 12).

Semiconductor offered that "ON Semiconductor would be pleased to provide Samsung with a nonexclusive license." (*Id.*). ON Semiconductor concluded by offering to travel to Korea (where Samsung's principal place of business is located) to "discuss these patents in more detail as well as the details of a suitable licensing arrangement." (*Id.*).

In response to ON Semiconductor's letter, Samsung and ON Semiconductor began negotiations for a potential license to the '594 and '644 patents. These negotiations included meetings in December 2005 and in February 2006. (Botsch Dec. ¶¶ 4-7). During these meetings, both ON Semiconductor and Samsung presented different "suggested construction[s]" and analysis of relevant claims, and considered the other party's proposals. (*Id.*; Exs. 2-5). Contrary to the Muir allegations (D.I. 12 ¶7), Mr. Botsch did not state that "they would select their litigation targets carefully," nor did any ON Semiconductor representative even mention, let alone threaten, litigation at either of these meetings. (Botsch Dec. ¶¶ 5-7; Cave Dec. ¶¶ 2-3).

On April 24, 2006, ON Semiconductor sent a second letter to Samsung to initiate negotiations for a potential license of the '001 patent. (Botsch Dec. ¶ 8, Ex. 6). ON Semiconductor suggested that the "'001 Patent is of interest" to Samsung and that the parties "continue our discussions about a suitable licensing arrangement in the near future." (*Id.* at Ex. 6). ON Semiconductor also referenced the ongoing negotiations regarding the '594 and '644 patents, stating "[i]t was good to speak to you last week about resolving our discussion, and we hope to reach an amicable resolution soon." (*Id.*). ON Semiconductor closed by inviting Samsung to contact it "if you have any questions in the meantime." (*Id.*). Samsung responded the same day, stating "[w]e'll take a look and get back to you." (*Id.*).

C. Licensing Negotiations Continue, And ON Semiconductor Makes Its First Offer.

Discussions between Samsung and ON Semiconductor continued regarding these and other patents that Samsung was interested in purchasing from ON Semiconductor continued through the end of July. (*Id.* at ¶ 10). The parties met again on August 16, 2006 for continued discussions directed to a potential license for the '594, '644, and '001 patents. (*Id.* at ¶ 11). ON Semiconductor proposed [redacted] (*Id.* at ¶ 12, Ex. 8). ON Semiconductor encouraged the parties "to move quickly and decisively to achieve final amicable resolution." (*Id.* at Ex. 8). As often happens with first offers in negotiations, Samsung said that it did not find this offer acceptable. (*Id.* at ¶ 12). Samsung did not make a counteroffer, however. (*Id.*). ON Semiconductor stated that it wanted to negotiate a resolution to this matter and did not want to litigate, but that ON Semiconductor did not intend to abandon its patent rights. (*Id.*).

When ON Semiconductor did not receive a substantive response to its offer, it sent a follow-up letter on September 6, 2006. (*Id.* at ¶ 13, Ex. 9). ON Semiconductor advised Samsung that if "Samsung intends to ignore ON's proposal and abandon any further discussions to resolve the underlying patent issues . . . then we must reemphasize to you that Samsung's decision will lead ON to pursue other paths to enforce its legal rights and remedies." (*Id.* at Ex. 9). It also assured Samsung, however, that ON Semiconductor "prefer[red] to follow the current path of professional and amicable negotiation with Samsung." (*Id.*). ON Semiconductor closed the letter by suggesting that "the parties get together again very shortly to review this matter and

determine which path to resolution will be followed going forward," and offered to meet Samsung in either Korea or the United States. (*Id.*).

On September 15, 2006, ON Semiconductor's Mr. Botsch called Samsung's Mr. Muir to ensure that Samsung had received ON Semiconductor's September 6, 2006 letter. (*Id.* at ¶ 14). Mr. Muir said that he had received the letter. Mr. Botsch responded that ON Semiconductor wanted to set up another meeting, and offered to meet in Korea during the third week of November. Mr. Muir's allegation that Mr. Botsch told him that "Defendants were considering filing a federal court litigation or an ITC proceeding against Samsung," (D.I. 12 ¶12), is flatly wrong. Mr. Botsch denies making any such statement. (Botsch Dec. ¶ 14).

As a result of the September 15, 2006 call, the parties had a fourth meeting to discuss in person the potential license agreement on September 29, 2006 in Korea, in which Samsung was represented by Mr. Shim, Mr. Lee, and one other local Korean Samsung representative, and ON Semiconductor was represented by Mr. Botsch. (*Id.* at ¶ 15). At this meeting, Mr. Shim stated on behalf of Samsung that "I want to give value to your patents," and that Samsung would prefer [redacted] at the August 16, 2006 meeting. (*Id.* at ¶16). Mr. Botsch responded that [redacted] could be acceptable to ON Semiconductor, but that ON Semiconductor wanted to hear a specific number. Mr. Shim said that he was "not prepared to do that today." (*Id.*). The parties agreed to meet again with both parties prepared to discuss concrete terms of an agreement. (*Id.*). ON Semiconductor reiterated that, because ON Semiconductor had made the only offer to date, it wanted to hear a specific counteroffer from Samsung. (*Id.*).

The parties arranged to meet again in Texas on November 28, 2006. (*Id.* at ¶17, Ex. 10). When Samsung made clear that it would not respond to ON Semiconductor's August

16, 2006 proposal by making a counteroffer, however, the parties scheduled a telephone meeting instead of an in-person meeting on November 28, 2006. (*Id.* at ¶¶ 18-20, Exs. 11-13).

D. ON Semiconductor Makes A Second Offer, Samsung Claims To Consider The Offer, And Both Parties Reaffirm Their Commitment To Amicable Resolution.

On November 28, 2006, ON Semiconductor's Mr. Cave and Mr. Botsch had a telephonic meeting with Mr. Shim. (*Id.* at ¶¶ 21-22; Cave Dec. ¶ 4). Mr. Shim said that he was the only Samsung representative on this call. (Botsch Dec. ¶ 21; Cave Dec. ¶ 4). They discussed the ongoing negotiations between ON Semiconductor and Samsung regarding licensing of the '594, '644, and '001 patents. (Cave Dec. ¶ 4). Mr. Shim stated twice during this meeting that Samsung did "not want to litigate." (Botsch Dec. ¶ 22; Cave Dec. ¶ 4). Mr. Cave and Mr. Botsch assured Mr. Shim that ON Semiconductor also preferred not to litigate the matter, and was seeking a business agreement. (Botsch Dec. ¶ 22; Cave Dec. ¶ 4).

Mr. Cave made an alternative proposal during the November 28 meeting, [redacted] in a good-faith effort to advance the negotiations. (Botsch Dec. ¶ 22; Cave Dec. ¶ 5). Mr. Cave proposed [redacted] (Botsch Dec. ¶ 22; Cave Dec. ¶ 5). This represented [redacted] (Botsch Dec. ¶ 22; Cave Dec. ¶ 5). Mr. Cave added that ON Semiconductor would entertain a counterproposal from Samsung [redacted] (Botsch Dec. ¶ 22; Cave Dec. ¶5). Mr. Shim, who was in the United States at that time, responded that he would think about it and that he needed to talk to "my management and my board" in Korea to get

"approval" and would call ON Semiconductor the next day. (Botsch Dec. ¶ 23; Cave Dec. ¶ 6). Mr. Shim gave no indication that he found ON Semiconductor's offer unreasonable or too high; and ON Semiconductor believed the fact that Mr. Shim said he was seeking board approval before responding indicated that Mr. Shim hoped to accept ON Semiconductor's offer or at least to finally make a counteroffer. (Botsch Dec. ¶ 23; Cave Dec. ¶ 6). Further, Samsung had previously informed ON Semiconductor that [redacted] was acceptable to Samsung in principle, as Mr. Muir admits. (D.I. 12 ¶ 15).

On November 29, Mr. Shim called Mr. Botsch and advised him that he had not yet been able to contact the "right people" in Korea, but that he planned to do so that evening, and would call Mr. Botsch the next day around 5 or 6 p.m. (Botsch Dec. ¶ 24). Mr. Shim also asked whether Mr. Botsch and Mr. Cave would be available for a face-to-face meeting in Dallas on December 1st, two days later. Mr. Botsch said he would be available and would check on Mr. Cave's availability. (*Id.*).

E. Negotiations Continue As Samsung Responds To ON Semiconductor's Offer By Filing A Declaratory Judgment Action And Making A Counteroffer.

On November 30, around 5:30 p.m. local Arizona time, just two days after ON Semiconductor had made its latest offer to Samsung, and more significantly, two days after both parties had assured each other that they did not have any present intent or desire to litigate these patents and Mr. Shim expressed a desire to meet again, Mr. Shim called Mr. Botsch to advise for the first time that the parties were "very far apart," and as a result, that Samsung had filed a declaratory judgment action against ON Semiconductor regarding the '594, '644, and '001 patents, which were the subject of the parties' negotiations. (*Id.* at ¶ 25).

Notably, Mr. Muir concedes that at the time Samsung filed its suit on November 30, "[n]either Mr. Botsch nor any of Defendants' other representatives indicated that Defendants

planned to file suit against Samsung within a specific or definite timeframe, nor did they ever indicate that they were considering bringing suit in the Eastern District of Texas." (D.I. 12 ¶ 16).

Mr. Shim told Mr. Botsch that Samsung was withholding service of process because "it did not want to go down the litigation path" and hoped to settle the matter directly with ON Semiconductor. (Botsch Dec. ¶ 25). Mr. Shim followed this statement with Samsung's first counteroffer proposal, [redacted] (*Id.* at ¶¶ 25-26).

The same day, after 6:00 p.m., local Arizona time, Mr. Cave called Mr. Shim. (Cave Dec. ¶ 7). Mr. Cave advised that he had heard that Samsung had sued ON Semiconductor, and asked Mr. Shim to confirm this information, because he found it hard to believe given Mr. Shim's recent assurances. (*Id.*). Mr. Shim responded that it was "just a D.J." and that it had only been filed because Samsung "needed protection," and that Mr. Cave should not get "too excited" about it. (*Id.*). Mr. Cave repeated his request that Mr. Shim confirm that Samsung had sued ON Semiconductor and Mr. Shim again discounted the action. (*Id.* at ¶ 8). After a third request, Mr. Shim finally confirmed that Samsung had filed the complaint that listed Samsung as plaintiff and ON Semiconductor as defendant. (*Id.* at ¶ 9).

Two business days later, on Monday, December 4, 2006, ON Semiconductor filed a direct action in the Eastern District of Texas against Samsung and the Samsung affiliates, alleging that these defendants infringe the '594, '644, and '001 patents, as well as the '827 patent. (Ex. A). ON Semiconductor served process on each of the defendants the same day.

(Ex. B). On December 6, two days later, Samsung served process on ON Semiconductor in this Delaware action. (D.I. 5-6).

F. Samsung's Allegations In The Complaint Concerning The Basis For Its "Reasonable Apprehension of Suit."

Samsung's complaint alleges that ON Semiconductor "has accused Samsung of infringing" the patents in suit. (D.I. 1 at ¶¶ 13, 20, 27). It further alleges that ON Semiconductor "demanded . . . exorbitant sums of money" and had "informed Samsung that it will not go away unless Samsung enters into a patent license with ON Semiconductor." (*Id.* at ¶¶ 14, 21, 28).[4] From these allegations, Samsung concludes that it had "a reasonable apprehension of suit." (*Id.* at ¶¶ 15, 22, 29).

ARGUMENT

Samsung's November 30, 2006 declaratory judgment complaint does not meet the basic statutory requirement of raising an "actual controversy" because, at the time Samsung filed this action, it had no objectively reasonable apprehension of an imminent suit by ON Semiconductor. Quite to the contrary, just two days before, both parties had reconfirmed their intention to continue negotiations, and Samsung had requested another meeting. Even if the Court were to find an actual controversy, it should decline to hear the matter because the filing of this action was an abuse of the Declaratory Judgment Act, a factor this Court has broad discretion to consider. Similarly, allowing this action to proceed would contravene sound

[4] In its amended complaint, Samsung additionally alleges that ON Semiconductor "made good on its threats of litigation" by filing its Texas action. (D.I. 8 at ¶¶ 26, 36, 46). As even Samsung's own declarant concedes, there was no threat by ON Semiconductor of any imminent suit when Samsung filed this action. (*See* D.I. 12 at ¶ 12). Moreover, as will be discussed further in the Argument section below, there must be an actual controversy *at the time the case is filed* and Samsung cannot create jurisdiction *nunc pro tunc* by pointing to subsequent actions in an amended complaint.

judicial administration by discouraging pre-litigation licensing attempts and by rewarding the bad-faith negotiating tactics of Samsung.

A. This Court Lacks Jurisdiction To Hear The Declaratory Judgment Claims Because There Was No Actual Controversy When Samsung Filed This Action.

The Declaratory Judgment Act "only supports jurisdiction in the event of an 'actual controversy.'" *Gen-Probe Inc. v. Vysis, Inc.*, 359 F.3d 1376, 1379 (Fed. Cir. 2004) (quoting 28 U.S.C § 2201(a)); *see also GAF Bldg.*, 90 F.3d at 481 ("[T]he existence of an actual controversy is an absolute predicate for declaratory judgment jurisdiction."); *BP Chems. Ltd. v. Union Carbide Corp.*, 4 F.3d 975, 977 (Fed. Cir. 1993) ("There must be a 'definite and concrete' dispute between adverse parties, appropriate to immediate and definitive determination of their legal rights.").[5]

Proof of an actual controversy requires both: (1) "*an explicit threat or other action by the patentee*, which creates a *reasonable apprehension* on the part of the declaratory relief plaintiff that it will face an infringement suit;" and (2) "present activity which could constitute infringement or concrete steps taken with the intent to conduct such activity." *BP Chems.*, 4 F.3d at 978 (emphasis added). Only the first prong is at issue here.

A reasonable apprehension of suit must be based on objective circumstances present at the time the suit is filed. A "subjective apprehension of an infringement suit is insufficient to satisfy the actual controversy requirement." *Indium Corp. of Am. v. Semi-Alloys, Inc.*, 781 F.2d 879, 883 (Fed. Cir. 1985); *see also Cygnus Therapeutic Sys. v. ALZA Corp.*, 92 F.3d 1153, 1160 (Fed. Cir. 1996), *overruled on other grounds by Nobelpharma Ab v. Implant*

---

[5] In patent cases, Federal Circuit law applies to the question whether an actual controversy exists with respect to actions seeking a declaration of non-infringement and/or invalidity. *See, e.g., Shell Oil Co. v. Amoco Corp.*, 970 F.2d 885, 888 n.4 (Fed. Cir. 1992).

Innovations, Inc., 141 F.3d 1059 (Fed. Cir. 1998) ("[T]he 'reasonable apprehension of suit' test requires more than the nervous state of mind of a possible infringer; it requires that the objective circumstances support such an apprehension."). The Federal Circuit recently held that, when a declaratory judgment action is filed, the declaratory plaintiff must not only have a reasonable apprehension that the patentee will sue it for infringement, but also that the lawsuit is "*imminent*." *Teva Pharms. USA, Inc. v. Pfizer Inc.*, 395 F.3d 1324, 1333 (Fed. Cir. 2005).

Although a court normally considers the facts alleged in the complaint to be true and correct when ruling on a motion to dismiss for lack of subject matter jurisdiction, when such a motion "challenges the truth of jurisdictional facts alleged in the complaint," as the current motion does, a court "may consider relevant evidence" to resolve the dispute. *Reynolds v. Army & Air Force Exch. Serv.*, 846 F.2d 746, 747 (Fed. Cir. 1988); *see also Mortensen v. First Fed. Sav. & Loan Ass'n*, 549 F.2d 884, 891 (3d Cir. 1977) ("Because at issue in a factual 12(b)(1) motion is the trial court's jurisdiction—its very power to hear the case—there is substantial authority that the trial court is free to weigh the evidence and satisfy itself as to the existence of its power to hear the case."). Samsung bears the burden of establishing an objectively reasonable apprehension of suit based on the "totality of the circumstances." *Gen-Probe,* 359 F.3d at 1379.

1. Samsung Had No Objectively Reasonable Apprehension Of Imminent Suit.

Samsung's Mr. Shim told ON Semiconductor executives that it had filed the instant suit not because of any apprehension of imminent suit, but because it "needed protection." (Cave Dec. ¶ 7). At the same time, Mr. Shim made a counteroffer — confirming that the negotiations were still ongoing — and said Samsung was not going to serve its complaint because "it did not want to go down the litigation path." (Botsch Dec. ¶¶ 25-26). Indeed, Samsung dismissively referred to this action as "just a D.J." that was nothing to get "excited"

about. (Cave Dec. ¶ 7). Samsung's Mr. Muir admitted that neither Mr. Botsch nor any other ON Semiconductor representative "had indicated that Defendants planned to file suit against Samsung within a specific or definite timeframe," (D.I. 12 ¶16), thus demonstrating that Samsung did *not* reasonably apprehend an imminent suit.

Far from informing ON Semiconductor that Samsung would not pay ON Semiconductor the "exorbitant sums that it [was] seeking," (D.I. 1 ¶¶ 14, 21, 28), Samsung said it was checking with its "management and board" and that it would respond to ON Semiconductor's offer the following day. (Botsch Dec. ¶ 23; Cave Dec. ¶ 6). On November 29, during a follow-up call from Samsung's representative Mr. Shim to Mr. Botsch, Samsung again did *not* reject the pending offer but rather Mr. Shim stated that he was trying to speak to the "right people" in Korea and would respond the following day, and asked for a face-to-face meeting in Dallas on December 1. (Botsch Dec. ¶ 24). Instead, Samsung filed this action. This conduct shows Samsung had no apprehension of an imminent suit, but rather was stalling for time so it could secretly file a complaint as a tactical maneuver to gain leverage in the ongoing licensing negotiations.

2. Samsung Cannot Prove That ON Semiconductor Made Any Express Threats Or Took Other Action That Created A Reasonable Apprehension.

The only actions that Samsung has cited as the basis for this action are that ON Semiconductor accused Samsung of infringing its patents, demanded Samsung license its patents "for exorbitant sums of money," and "informed Samsung that it will not go away unless Samsung enters into a patent license with ON Semiconductor." (D.I. 1 ¶¶ 13, 14, 15, 20, 21, 22, 27, 28, 29). None of Samsung's allegations, even if accepted as true, amount to an actual controversy for several reasons.

First, Samsung does not allege that ON Semiconductor expressly threatened litigation regarding the '594, '644, or '001 patents, or even implied that litigation was imminent. Nor could it. Just two days before Samsung filed this action, ON Semiconductor explicitly reassured Samsung that it "preferred not to litigate the matter, and *was seeking a business agreement*." (Botsch Dec. ¶ 22; Cave Dec. ¶ 4 (emphasis added)).

Second, as the Federal Circuit has repeatedly held, neither an offer of a patent license, nor language in a letter stating that the declaratory judgment plaintiff's product is "covered by" or "appears to infringe" the defendant's patents, amounts to an actual controversy. *Phillips Plastics Corp. v. Kato Hatsujou Kabushiki Kaisha*, 57 F.3d 1051, 1053 (Fed. Cir. 1995) ("[T]he offer of a patent license does not create an actual controversy); *EMC Corp. v. Norand Corp.*, 89 F.3d 807, 811 (Fed. Cir. 1996) ("[A] patentee's offer of a license, without more, is insufficient to establish the predicate for declaratory judgment jurisdiction."). *See also Vermeer Mfg. Co. v. Deere & Co.*, 379 F. Supp. 2d 645, 649-50 (D. Del. 2005) (finding patentee's statements that plaintiff's product "appears to infringe" and that patentee "will enforce its patent rights" insufficient to create a reasonable apprehension of suit); *DuPont Dow Elastomers, L.L.C. v. Greene Tweed of Delaware, Inc.*, 148 F. Supp. 2d 412, 413 (D. Del. 2001) (finding an allegation that plaintiff's products "may be infringing" did not amount to an express threat to sue).

Once ON Semiconductor believed that Samsung's products were covered by its patents, it engaged Samsung in negotiations, offering a license. ON Semiconductor expressed its continued desire to negotiate a license in its September 6, 2006 letter to Samsung, saying that, while it reserved its right "to pursue other paths to enforce its legal rights" if Samsung were to abandon further discussions, it "prefer[ed] to follow the *current path of professional and*

amicable negotiation with Samsung." (Botsch Dec. Ex. 9 (emphasis added)). No one could have reasonably perceived this statement as indicating that ON Semiconductor was threatening — imminently or otherwise — to sue Samsung. To the contrary, Samsung never abandoned its attempts to negotiate with ON Semiconductor. *See Fresenius USA, Inc. v. Transonic Sys., Inc.*, 207 F. Supp. 2d 1009, 1012 (N.D. Cal. 2001) (holding it was "objectively unreasonable" for plaintiff to fear imminent suit while negotiations were still ongoing because, even though the patentee threatened to sue, that threat was conditioned on negotiations failing); *see also EMC*, 89 F.3d at 811 ("The threat of enforcement . . . is the entire source of the patentee's bargaining power.").

Third, throughout the negotiations leading up to the filing of this suit, ON Semiconductor was clear that it intended to reach an amicable solution. (*See, e.g.*, Botsch Dec. Ex. 1 ("I will be contacting you in the near future to discuss potential dates for a meeting . . . in which we can discuss these patents in more detail as well as the details of a suitable licensing arrangement."), Ex. 6 ("It was good to speak with you last week about resolving our discussion, and we hope to reach an amicable resolution soon."), Ex. 8 ("Need to move quickly and decisively to achieve a final amicable resolution.")).

Fourth, as this court and the Federal Circuit have recognized, the fact that negotiations were still ongoing at the time of filing itself demonstrates that Samsung could not objectively have reasonably apprehended an imminent suit. *EMC*, 89 F.3d at 811 (finding "proposed or ongoing license negotiations" are insufficient for declaratory judgment jurisdiction); *Phillips Plastics*, 57 F.3d at 1053-54 (affirming dismissal of a declaratory judgment action because negotiations were ongoing and the patentee "was seeking a commercial, not a judicial remedy"); *Vermeer*, 379 F. Supp. 2d at 649-50 (dismissing declaratory judgment action

where "[t]he record . . . demonstrates that negotiations were still ongoing when suit was filed"); *see also Livorsi Marine, Inc. v. Nordskog Publishing, Inc.*, 268 F. Supp. 2d 994, 998 (N.D. Ill. 2003) ("[W]hen parties are still engaged in licensing negotiations as of the filing date of an action for declaratory judgment, there can be no actual controversy.").

ON Semiconductor's open and unanswered negotiation proposals, such as the proposal and simultaneous invitation for a counterproposal to which Samsung said it would respond (*see* Botsch Dec. ¶¶ 22-23; Cave Dec. ¶¶ 5-6), Samsung's request for a meeting the day before it filed (Botsch Dec. ¶24), and its withholding of service followed by its attempts to negotiate a licensing solution *after* filing a declaratory action (*id.* at ¶¶ 25-26), are proof that negotiations were ongoing. *See, e.g., Vermeer*, 379 F. Supp. 2d at 648-49 (finding negotiations ongoing where declaratory plaintiff sent a letter to the defendant the day after filing the declaratory action, explaining that the suit "was 'in the nature of possible settlement discussions' and that 'Vermeer would be amenable to listening to any Deere counterproposals . . . before proceed[ing] with service of the complaint and institution of the lawsuit'").

To the extent that Samsung bases its alleged apprehension of suit on how ON Semiconductor *might* have responded to the counteroffer that Samsung was *contemplating* but had not yet made, such an argument is improper and irrelevant. Samsung must demonstrate an objectively reasonable apprehension of suit arising from ON Semiconductor's actual conduct, not speculation as to how ON Semiconductor might respond to a counteroffer Samsung had not yet made. *BP Chems.*, 4 F.3d at 977 ("The controversy must be actual, not hypothetical or of uncertain prospective occurrence."); *see also Shell Oil*, 970 F.2d at 889 (finding the Declaratory Judgment Act is intended "to protect *threatened* parties, not to drag a *non-threatening* patentee

into court") (emphasis added). Accordingly, when viewed in their totality, the "objective circumstances" here do not support a reasonable apprehension of suit.

3. Whether Samsung Had An Objectively Reasonable Apprehension Of Imminent Suit Must Be Based On The Existing Facts At The Time Suit Was Filed.

Samsung cannot avoid the fact that it lacked the requisite objectively "reasonable apprehension" when it filed its declaratory judgment action by pointing to ON Semiconductor's later direct action in Texas. "The presence or absence of a case or controversy is based on facts at the time the complaint was filed." *MedImmune, Inc. v. Centocor, Inc.*, 409 F.3d 1376, 1381 (Fed. Cir. 2005) (citing *GAF Bldg.*, 90 F.3d at 483 ("Later events may not create jurisdiction where none existed at the time of filing."). *See also Fairplay Elec. Cars, LLC v. Textron Innovations, Inc.*, 431 F. Supp. 2d 491, 493 (D. Del. 2006) (declaratory judgment plaintiff cannot rely on letter sent after action was filed). Thus, a patentee's decision to later file a direct action is irrelevant to whether the declaratory plaintiff had a reasonable apprehension when it filed its anticipatory suit. *MedImmune*, 409 F.3d at 1381 (holding a patentee's later-filed infringement action is irrelevant to whether a reasonable apprehension of suit existed because "the presence or absence of a case or controversy is based on facts at the time the complaint was filed").

Because Samsung did not have, and could not have had, a reasonable apprehension of suit at a time when the parties' negotiations were ongoing, this Court should dismiss Samsung's November 30, 2006 declaratory judgment complaint for lack of subject matter jurisdiction under Fed. R. Civ. P. 12(b)(1).

B. This Court Should Exercise Its Discretion To Dismiss This Declaratory Judgment Action.

Even where an actual controversy is shown to exist, courts are not required to hear declaratory judgment actions, but rather, in their discretion "*may*" chose to consider and rule

on the action. 28 U.S.C § 2201(a) (emphasis added); *Wilton v. Seven Falls Co.,* 515 U.S. 277, 286-87 (1995). The Declaratory Judgment statute "specifically entrusts courts with discretion to hear declaratory suits *or not* depending on the circumstances." *Serco Servs. Co. LP. v. Kelley Co. Inc.*, 51 F.3d 1037, 1039 (Fed. Cir. 1995) (emphasis added). "[T]he court has *broad discretion* to refuse to entertain a declaratory judgment action." *EMC*, 89 F.3d at 813-14 (emphasis added). In fact, this Court's discretion to hear or not hear a declaratory judgment suit is so broad that the Supreme Court has explained that "the statute's textual commitment to discretion, and the breadth of leeway we have always understood it to suggest, distinguish the declaratory judgment context from other areas of law in the which concepts of discretion surface." *Wilton,* 515 U.S. at 286-87.

A district court should only entertain declaratory judgment actions, even where an actual controversy exists, where the exercise of jurisdiction comports with "[1] the purposes of the Declaratory Judgment Act and [2] the principles of sound judicial administration." *EMC,* 89 F.3d at 813-14; *see also Wilton,* 515 U.S. at 288 ("In the declaratory judgment context, the normal principle that federal courts should adjudicate claims within their jurisdiction yields to considerations of practically and wise judicial administration."); *Serco Servs.*, 51 F.3d at 1039 (noting district courts should "make a reasoned judgment whether the investment of time and resources will be worthwhile" before exercising discretion to hear a declaratory judgment claim).

The Court should dismiss Samsung's declaratory judgment claims because exercising jurisdiction here would neither be consistent with the purposes of the Declaratory Judgment Act, nor with the principles of sound judicial administration.

1. Samsung Misused The Declaratory Judgment Device To Gain Negotiating Leverage.

The purpose of the Declaratory Judgment Act is to permit a party to a dispute to initiate legal action where the "interests of [the other] side to the dispute may be served by delay in taking legal action." *BP Chems.*, 4 F.3d at 977. The Federal Circuit has described "the type of situation the Declaratory Judgment Act was intended to address" as follows:

> [A] patent owner engages in a *danse macabre*, brandishing a Damoclean threat with a sheathed sword . . . Guerilla-like, the patent owner attempts extra-judicial patent enforcement with scare-the-customer-and-run tactics that infect the competitive environment of the business community with uncertainty and insecurity.

EMC, 89 F.3d at 814-15 (quoting *Arrowhead*, 846 F.2d at 734-35). This is not such a case. By contrast, where a party files a declaratory action as "a tactical measure filed in order to improve [declaratory plaintiff's] posture in . . . ongoing negotiations," the purposes of this Act have been abused. *Id.* at 815. Courts properly dismiss cases brought for such tactical purposes. *Id.*

In *EMC Corp.*, a case with facts strikingly similar to those here, the Federal Circuit affirmed the district court's dismissal of the declaratory judgment action. There, the parties were engaged in negotiations "up to the time the complaint was filed," the patentee was not using the negotiations merely as "a pretext designed to give [patentee] a basis for keeping [declaratory plaintiff] from obtaining declaratory judgment relief," and the declaratory plaintiff called the patentee the day after it filed suit explaining that it "just thought it was in their interest to protect themselves first and continue discussions." *Id.* at 815. The Federal Circuit held, under these facts, the district court properly "view[ed] the declaratory judgment complaint as a tactical measure filed in order to improve EMC's posture in the ongoing negotiations," and thus, the suit did not serve the purposes of the Declaratory Judgment Act. *Id.* at 815.

Similarly, here, the negotiations between Samsung and ON Semiconductor were ongoing up to, and even past, the time Samsung filed its complaint. Samsung intentionally kept the negotiations open, telling ON Semiconductor only days before it filed that it did not want to litigate, that it would consider ON Semiconductor's offer, and that it wanted another meeting. (Botsch Dec. ¶¶ 22-24; Cave Dec. ¶¶ 4-6). Indeed, Samsung extended a counteroffer even ***after*** it filed its complaint. (Botsch Dec. ¶¶ 25-26). Further, there is no allegation that ON Semiconductor participated in negotiations with Samsung merely as a pretext to prevent Samsung from filing a declaratory judgment action. To the contrary, ON Semiconductor attempted in good faith to resolve the matter through negotiation, including revising its proposal several times and specifically inviting a counteroffer from Samsung (*id.* at ¶ 22; Cave Dec. ¶ 5), had offered to meet with Samsung in Korea several times (Botsch Dec. Exs. 1, 9), and once even offered to send ON Semiconductor's general counsel to Korea to meet at Samsung's convenience (*id.* at Ex. 6). Finally, like the declaratory plaintiff in *EMC*, Mr. Shim told Mr. Cave the day Samsung filed its complaint that it was "only a D.J.," that Samsung had merely filed it as "protection," and hoped that negotiations would continue. (Botsch Dec. ¶ 25; Cave Dec. ¶ 7). *See EMC*, 89 F.3d at 815 (declaratory judgment plaintiff "just thought it was in their interest to protect themselves first and continue discussions").

While these facts alone show that Samsung was the party that was engaged in the *danse macabre*, and that it filed this action to gain tactical leverage in negotiations as described in *EMC*, Samsung's lack of good faith is further revealed by Mr. Shim's assurances that he would respond to ON Semiconductor's offers and his request that Messrs. Botsch and Cave check their schedules for a proposed meeting on December 1, while Samsung surreptitiously filed this suit in the interim. (*See* Botsch Dec. ¶ 24). ***After*** Samsung informed ON

Semiconductor that it had filed this action, and ***after*** Samsung specifically noted that it was withholding service in the hope of an out of court resolution, Samsung ***only then*** made a counteroffer [redacted] (Botsch Dec. ¶¶ 25-26). Allowing an action brought in bad faith and for such reasons to proceed would "abuse the declaratory judgment device." *EMC* 89 F.3d at 814. The Court should exercise its broad discretion to dismiss this declaratory judgment action.

2. Exercising Jurisdiction Over This Declaratory Judgment Action Would Punish ON Semiconductor For Reasonably Pursuing Negotiation Rather Than Litigation, Contrary To The Principles Of Sound Judicial Administration.

In addition to upholding the purposes of the Declaratory Judgment Act, courts also should dismiss declaratory actions where necessary to protect "the principles of sound judicial administration." *EMC,* 89 F.3d at 813-14. *See also Wilton,* 515 U.S. at 288 ("In the declaratory judgment context, the normal principle that federal courts should adjudicate claims within their jurisdiction yields to considerations of practicality and wise judicial administration"); *Kerotest Mfg. Co. v. C-O-Two Fire Equipment Co.*, 342 U.S. 180, 183 (1952). Notably, the "factors relevant to wise administration here are equitable in nature." *Kerotest*, 342 U.S. at 183. One important equitable consideration is that "[p]otential plaintiffs should be encouraged to attempt settlement discussions (in good faith and with dispatch) prior to filing lawsuits without fear that the defendant will be permitted to take advantage of the opportunity to institute litigation in a district of its own choosing." *Davox Corp. v. Digital Sys. Int'l, Inc.*, 846 F. Supp. 144, 148 (D. Mass. 1993) (quoting *Columbia Pictures Indus., Inc. v. Schneider*, 435 F. Supp. 742, 747 (S.D.N.Y. 1977), *aff'd,* 573 F.2d 1288 (2d Cir. N.Y. 1978)).

Courts have deemed encouraging attempts at settlement to be more important than deferring to any first filed lawsuit, because declaratory plaintiffs "should not be permitted to take

advantage of the fact that [patentee] reasonably deferred filing potentially protracted and expensive litigation, and indeed, was perhaps misled into believing it would not be prejudiced by doing so by [declaratory plaintiff's] response to its" negotiation attempts. *Davox Corp.*, 846 F. Supp. at 148. Indeed, while "[t]he general rule [of wise judicial administration] favors the forum of the first-filed action, whether or not it is a declaratory action[, e]xceptions . . . are not rare, and are made when justice or expediency requires." *Genentech, Inc. v. Eli Lilly and Co.*, 998 F.2d 931, 937 (Fed. Cir. 1993).

It is proper to dismiss or stay a declaratory action in favor of a later filed infringement action where the declaratory action was brought while the patentees pursued good faith negotiations, because a patentee "should not be deprived of its choice of forum merely because it attempted to arrange a settlement." *Metro Optics, Inc. v. Contex, Inc.*, No. 95-CV-2157-T, 1996 U.S. Dist. LEXIS 11081, at *4-5 (N.D. Tex. Mar. 14, 1996) (staying a declaratory action in favor of a later filed infringement action where declaratory plaintiff responded to patentee's negotiation overtures by stating that it would study the patent and respond in several weeks but instead filed a declaratory judgment action); *Davox Corp.*, 846 F. Supp. at 148 (dismissing a declaratory action in favor of later filed infringement suit where the declaratory plaintiff told the patentee that it would respond to its overture letters, but instead filed the declaratory action); *Columbia Pictures*, 435 F. Supp. at 747 (staying a declaratory judgment action in favor of a later filed infringement action in part because the declaratory action was brought while patentee was making good faith efforts to settle the matter without litigation). Although this Court has not yet faced a case with these facts, it has recognized that "[w]hether a party has filed a declaratory judgment action anticipatorily or in bad faith is a proper factor for the court to consider in deciding whether to dismiss a first filed action." *Matsushita Battery*

Indus. Co., v. Energy Conversion Devices, Inc., No. 96-101-SLR, 1996 U.S. Dist. LEXIS 8153, at *9 (D. Del. Apr. 23, 1996).

Here, wise judicial administration calls for the dismissal of this action in favor of the direct action ON Semiconductor filed in Texas. To permit this action to proceed over the Texas action would reward Samsung for its bad faith attempt to leverage the negotiations and punish ON Semiconductor for taking Samsung and its counsel at their word in pursuing a licensing arrangement. (*See, e.g.,* Botsch Dec. ¶ 25).

CONCLUSION

For the foregoing reasons, Samsung's November 30, 2006 complaint should be dismissed because Samsung cannot establish that it possessed an objectively reasonable apprehension of suit at the time it filed for declaratory judgment. In the alternative, the Court should decline to exercise jurisdiction because the purposes of the Declaratory Judgment Act and the principles of sound judicial administration would not be served by hearing this action.

Defendant ON Semiconductor's Motion to Dismiss should be granted.

MORRIS, NICHOLS, ARSHT & TUNNELL LLP

Karen Jacobs Louden

/s/ *Karen Jacobs Louden*

Karen Jacobs Louden (#2881)
1201 N. Market Street
P.O. Box 1347
Wilmington, DE 19899
(302) 658-9200
klouden@mnat.com
Attorneys for Defendants

Kenneth R. Adamo
JONES DAY
2727 North Harwood Street
Dallas, TX 75201-1515
(214) 220-3939

T. Gregory Lanier
Behrooz Shariati
JONES DAY
2882 Sand Hill Road, Suite 240
Menlo Park, CA 94025
(650) 739-3939

December 27, 2006

549954

PUBLIC VERSION - REDACTED

CERTIFICATE OF SERVICE

I, the undersigned, hereby certify that on December 27, 2006 I electronically filed the foregoing with the Clerk of the Court using CM/ECF, which will send notification of such filing(s) to the following:

Josy Ingersoll
jingersoll@ycst.com

John Shaw
jshaw@ycst.com

I also certify that copies were caused to be served on December 27, 2006 upon the following in the manner indicated:

BY HAND

Josy W. Ingersoll (#1088)
John W. Shaw (#3362)
Young, Conaway, Stargatt & Taylor, LLP
The Brandywine Building
1000 West Street, 17th Floor
P.O. Box 391
Wilmington, DE 19899

BY FEDERAL EXPRESS

John M. Desmarais
James E. Marina
Kirkland & Ellis LLP
153 East 53rd Street
New York, NY 10022

Karen Jacobs Louden

/s/ Karen Jacobs Louden
klouden@mnat.com

CERTIFICATE OF SERVICE

I, the undersigned, hereby certify that on January 8, 2007, I electronically filed the foregoing with the Clerk of the Court using CM/ECF, which will send notification of such filing(s) to the following:

Josy W. Ingersoll
John W. Shaw

I also certify that copies were caused to be served on January 8, 2007 upon the following in the manner indicated:

BY HAND

Josy W. Ingersoll
John W. Shaw
YOUNG, CONAWAY, STARGATT & TAYLOR LLP
The Brandywine Building
1000 West Street, 17th Flr.
Wilmington, DE 19899

BY FEDERAL EXPRESS

John M. Desmarais
James E. Marina
KIRKLAND & ELLIS
153 East 53rd Street
New York, NY 10022

/s/ Karen Jacobs Louden (#2881)

Karen Jacobs Louden
klouden@mnat.com

EXHIBIT A

UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
TYLER DIVISION

ON SEMICONDUCTOR CORPORATION, and SEMICONDUCTOR COMPONENTS INDUSTRIES, L.L.C.
Plaintiffs,

v.

SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG TELECOMMUNICATIONS AMERICA GENERAL, L.L.C., SAMSUNG SEMICONDUCTOR, INC., and SAMSUNG AUSTIN SEMICONDUCTOR, L.L.C.,
Defendants.

Civil Action No. 6:06cv523

COMPLAINT

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff ON Semiconductor Corp. ("ON Semiconductor") and plaintiff Semiconductor Components Industries, L.L.C. ("Semiconductor Components") (collectively, "Plaintiffs"), for their Complaint against defendants Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., Samsung Telecommunications America General, L.L.C., Samsung Semiconductor, Inc. and Samsung Austin Semiconductor, L.L.C. (collectively "Defendants"), state as follows.

THE PARTIES

1. Plaintiff ON Semiconductor is a Delaware corporation with its principal place of business at 5005 East McDowell Road, Phoenix, AZ 85008.

2. Plaintiff Semiconductor Components, a Delaware limited liability company with its principal place of business at 5005 East McDowell Road, Phoenix, AZ 85008, is the principal domestic operating subsidiary of ON Semiconductor, and does business under the name of ON Semiconductor.

3. On information and belief, Defendant Samsung Electronics Co., Ltd. ("SEC") is a corporation organized and existing under the laws of Republic of Korea with its principal place of business at Samsung Main Building, 250, Taepyong-ro 2-ka, Chung-ku, Seoul 100-742, South Korea. On information and belief, SEC manufactures and, in cooperation with its subsidiaries, markets throughout the world, including in this district and elsewhere in the United States, a variety of semiconductor products including dynamic random access memory ("DRAM") devices.

4. Defendant Samsung Electronics America, Inc. ("SEA") is a New York corporation with its principal place of business at 105 Challenger Road, Ridgefield Park, New Jersey 07660. On information and belief, SEA is a subsidiary of SEC and sells and otherwise markets, in this district and elsewhere in the United States, a variety of electronic and semiconductor products

5. Defendant Samsung Telecommunications America General, L.L.C. ("STA") is a Delaware limited liability company with its principal place of business at 1301 East Lookout Drive, Richardson, Texas 75082. On information and belief, STA is a subsidiary of SEC and sells and otherwise markets, in this district and elsewhere in the United States, a variety of electronic and semiconductor products.

6. Defendant Samsung Semiconductor, Inc. ("SSI") is a California corporation with its principal place of business at 3655 North First Street, San Jose, California 95134. On

information and belief, SSI is a subsidiary of SEC and sells and otherwise markets, in this district and elsewhere in the United States, a variety of electronic and semiconductor products.

7. On information and belief, Defendant Samsung Austin Semiconductor, L.L.C. ("SAS") is a Delaware limited liability company with its principal place of business at 12100 Samsung Boulevard, Austin, Texas 78754. On information and belief, SAS is a subsidiary of SEC and sells and otherwise markets, in this district and elsewhere in the United States, a variety of semiconductor products including DRAM devices.

JURISDICTION AND VENUE

8. This Court has subject matter jurisdiction pursuant to 28 U.S.C. §§ 1331 and 1338 because this action arises under the patent laws of the United States, including 35 U.S.C. § 271 *et seq.*

9. This Court has personal jurisdiction over each of the Defendants. The Defendants have had minimum contacts with this forum as a result of business regularly conducted within the State of Texas and within this district and specifically as a result of, at least, the Defendants' distribution network wherein Defendants place their products that infringe Semiconductor Component's patents within the stream of commerce, which stream is directed at this district as well as Texas, and by committing the tort of patent infringement and/or contributing to or inducing acts of patent infringement by others within Texas and this district.

10. Venue is proper in this district pursuant to 28 U.S.C. §§ 1391(b) and (c) and 1400(b) because Defendants have regularly conducted business in this judicial district and certain of the acts complained of herein occurred in this judicial district.

COUNT I – INFRINGEMENT OF U.S. PATENT NO. 5,563,594

11. The allegations contained in paragraphs 1 through 10 are incorporated by reference as if fully set herein.

12. United States Patent No. 5,563,594 ("the '594 patent"), entitled "Circuit and Method of Timing Data Transfers," was duly and legally issued by the United States Patent and Trademark Office on October 8, 1996. Plaintiffs hold all right and interest in the '594 patent, including the right to sue for past, present and future infringement. A copy of the '594 patent is attached hereto as Exhibit A.

13. Defendants are infringing the '594 patent under one or more sections of 35 U.S.C. § 271 in this judicial district and elsewhere in the United States by the manufacture, use, sale, offer for sale and/or importation into the United States of product(s) falling within the scope of one or more claims of the '594 patent.

14. On information and belief, Defendants also contribute to and/or induce the infringement of at least one claim of the '594 patent.

15. Plaintiffs have been damaged by Defendants' infringement of the '594 patent. Plaintiffs are entitled to recover from each of the Defendants the damages sustained by them as a result of each of the Defendants' wrongful acts.

16. Defendants' infringement of Semiconductor Component's exclusive rights under the '594 patent will continue to damage Plaintiffs' business, causing irreparable harm, for which there is no adequate remedy at law, unless each of the Defendants is enjoined by this Court.

17. Defendants have had actual knowledge of the '594 patent and their infringement is deliberate and willful, entitling Plaintiffs to increased damages under 35 U.S.C. § 284 and to attorney fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

COUNT II – INFRINGEMENT OF U.S. PATENT NO. 6,362,644

18. The allegations contained in paragraphs 1 through 17 are incorporated by reference as if fully set herein.

19. United States Patent No. 6,362,644 ("the '644 patent"), entitled "Programmable Termination for Integrated Circuits," was duly and legally issued by the United States Patent and Trademark Office on March 26, 2002. Plaintiffs hold all right and interest in the '644 patent, including the right to sue for past, present and future infringement. A copy of the '644 patent is attached hereto as Exhibit B.

20. Defendants are infringing the '644 patent under one or more sections of 35 U.S.C. § 271 in this judicial district and elsewhere in the United States by the manufacture, use, sale, offer for sale and/or importation into the United States of product(s) falling within the scope of one or more claims of the '644 patent.

21. On information and belief, Defendants also contribute to and/or induce the infringement of at least one claim of the '644 patent.

22. Plaintiffs have been damaged by Defendants' infringement of the '644 patent. Plaintiffs are entitled to recover from each of the Defendants the damages sustained by Plaintiffs as a result of each of the Defendants' wrongful acts.

23. Defendants' infringement of Semiconductor Component's exclusive rights under the '644 patent will continue to damage Plaintiffs' business, causing irreparable harm, for which there is no adequate remedy at law, unless each of the Defendants is enjoined by this Court.

24. Defendants have had actual knowledge of the '644 patent and their infringement is deliberate and willful, entitling Plaintiffs to increased damages under 35 U.S.C. § 284 and to attorney fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

COUNT III – INFRINGEMENT OF U.S. PATENT NO. 5,361,001

25. The allegations contained in paragraphs 1 through 24 are incorporated by reference as if fully set herein.

26. United States Patent No. 5,361,001 ("the '001 patent"), entitled "Circuit and Method of Previewing Analog Trimming," was duly and legally issued by the United States Patent and Trademark Office on November 1, 1994. Plaintiffs hold all right and interest in the '001 patent, including the right to sue for past, present and future infringement. A copy of the '001 patent is attached hereto as Exhibit C.

27. Defendants are infringing the '001 patent under one or more sections of 35 U.S.C. § 271 in this judicial district and elsewhere in the United States by the manufacture, use, sale, offer for sale and/or importation into the United States of product(s) falling within the scope of one or more claims of the '001 patent.

28. On information and belief, Defendants also contribute to and/or induce the infringement of at least one claim of the '001 patent.

29. Plaintiffs have been damaged by Defendants' infringement of the '001 patent. Plaintiffs are entitled to recover from each of the Defendants the damages sustained by Plaintiffs as a result of each of the Defendants' wrongful acts.

30. Defendants' infringement of Semiconductor Component's exclusive rights under the '001 patent will continue to damage Plaintiff's business, causing irreparable harm, for which there is no adequate remedy at law, unless each of the Defendants is enjoined by this Court.

31. Defendants have had actual knowledge of the '001 patent and their infringement is deliberate and willful, entitling Plaintiffs to increased damages under 35 U.S.C. § 284 and to attorney fees and costs incurred in prosecuting this action under 35 U.S.C. § 285.

COUNT IV – INFRINGEMENT OF U.S. PATENT NO. 5,000,827

32. The allegations contained in paragraphs 1 through 31 are incorporated by reference as if fully set herein.

33. United States Patent No. 5,000,827 ("the '827 patent"), entitled "Method and Apparatus for Adjusting Plating Solution Flow Characteristics at Substrate Cathode Periphery to Minimize Edge Effect," was duly and legally issued by the United States Patent and Trademark Office on March 19, 1991. Plaintiffs hold all right and interest in the '827 patent, including the right to sue for past, present and future infringement. A copy of the '827 patent is attached hereto as Exhibit D.

34. Defendants are infringing the '827 patent under one or more sections of 35 U.S.C. § 271 in this judicial district and elsewhere in the United States by the manufacture, use, sale, offer for sale and/or importation into the United States of product(s) falling within the scope of one or more claims of the '827 patent.

35. On information and belief, Defendants also contribute to and/or induce the infringement of at least one claim of the '827 patent.

36. Plaintiffs have been damaged by Defendants' infringement of the '827 patent. Plaintiffs are entitled to recover from each of the Defendants the damages sustained by Plaintiffs as a result of each of the Defendants' wrongful acts.

37. Defendants' infringement of Semiconductor Component's exclusive rights under the '827 patent will continue to damage Plaintiffs' business, causing irreparable harm, for which there is no adequate remedy at law, unless each of the Defendants is enjoined by this Court.

PRAYER FOR RELIEF

WHEREFORE, Plaintiffs pray for judgment in its favor against each of the Defendants, and requests the following relief:

A. An adjudication that Defendants have infringed, contributed to the infringement of, and/or induced infringement of the '594, '644, '001, and '827 patents;

B. An adjudication that the '594, '644, '001, and '827 patents are valid and enforceable;

C. An accounting of all damages sustained by Plaintiffs as a result of Defendants' acts of infringement;

D. An award to Plaintiffs of actual damages adequate to compensate them for Defendants' acts of direct, contributory, and/or inducement of infringement, together with prejudgment and post-judgment interest and costs;

E. An award to Plaintiffs of enhanced damages, up to and including trebling of Plaintiffs' damages, pursuant to 35 U.S.C. § 284 for Defendants' willful infringement;

F. A preliminary and permanent injunction order against further infringement of the '594, '644, '001 and '827 patents by each of the Defendants, their officers, agents, servants, employees, subsidiaries, and those persons acting in concert with it, including related individuals and entities, customers, representatives, manufacturers, OEMs, dealers, and distributors;

G. An award to Plaintiffs their costs and reasonable attorney fees incurred in this action as provided by 35 U.S.C. § 285; and

H. That the Court award such other relief as this Court deems just and proper.

JURY DEMAND

Pursuant to Federal Rule of Civil Procedure 38(b), Plaintiffs demand a trial by jury on all issues and claims so triable.

Date: December 4, 2006

Respectfully submitted,

Kenneth R. Adamo
State Bar No. 00846960
kradamo@jonesday.com
Hilda C. Galvan
State Bar No. 00787512
hcgalvan@jonesday.com
JONES DAY
2727 North Harwood Street
Dallas, Texas 75201-1515
Telephone: (214) 220-3939
Facsimile: (214) 969-5100

Tharan Gregory Lanier
tglanier@jonesday.com
CA Bar No. 138784
JONES DAY
2882 Sand Hill Road, Suite 240
Menlo Park, CA 94025
Telephone: (650) 739-3939
Facsimile: (650) 739-3900

Carl R. Roth
State Bar No. 17312000
cr@rothfirm.com
Michael C. Smith
ms@rothfirm.com
115 N Wellington Suite 200
P O Box 876
Marshall, Texas 75670
Telephone: (903) 935-1665
Facsimile: (903) 935-1797

ATTORNEYS FOR ON SEMICONDUCTOR CORPORATION AND SEMICONDUCTOR COMPONENTS INDUSTRIES, L.L.C.

Of Counsel:
Behrooz Shariati
JONES DAY
2882 Sand Hill Road, Suite 240
Menlo Park, CA 94025

EXHIBIT A

US005563594A

United States Patent [19]

Ford et al.

[11] Patent Number: 5,563,594

[45] Date of Patent: Oct. 8, 1996

[54] **CIRCUIT AND METHOD OF TIMING DATA TRANSFERS**

[75] Inventors: **David K. Ford**, Gilbert; **Bernard E. Weir, III**, Chandler, both of Ariz.

[73] Assignee: **Motorola**, Schaumburg, Ill.

[21] Appl. No.: **298,715**

[22] Filed: **Aug. 31, 1994**

[51] **Int. Cl.**[6] **H03M 9/00**

[52] **U.S. Cl.** **341/100**; 341/101; 327/279

[58] **Field of Search** 341/100, 101; 326/93; 327/160, 175, 265, 279

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,218,758	8/1980	Allen et al.	364/900
4,445,215	4/1984	Svendsen	370/279
4,815,107	3/1989	Kishimoto et al.	375/96
5,379,038	1/1995	Matsumoto	341/101

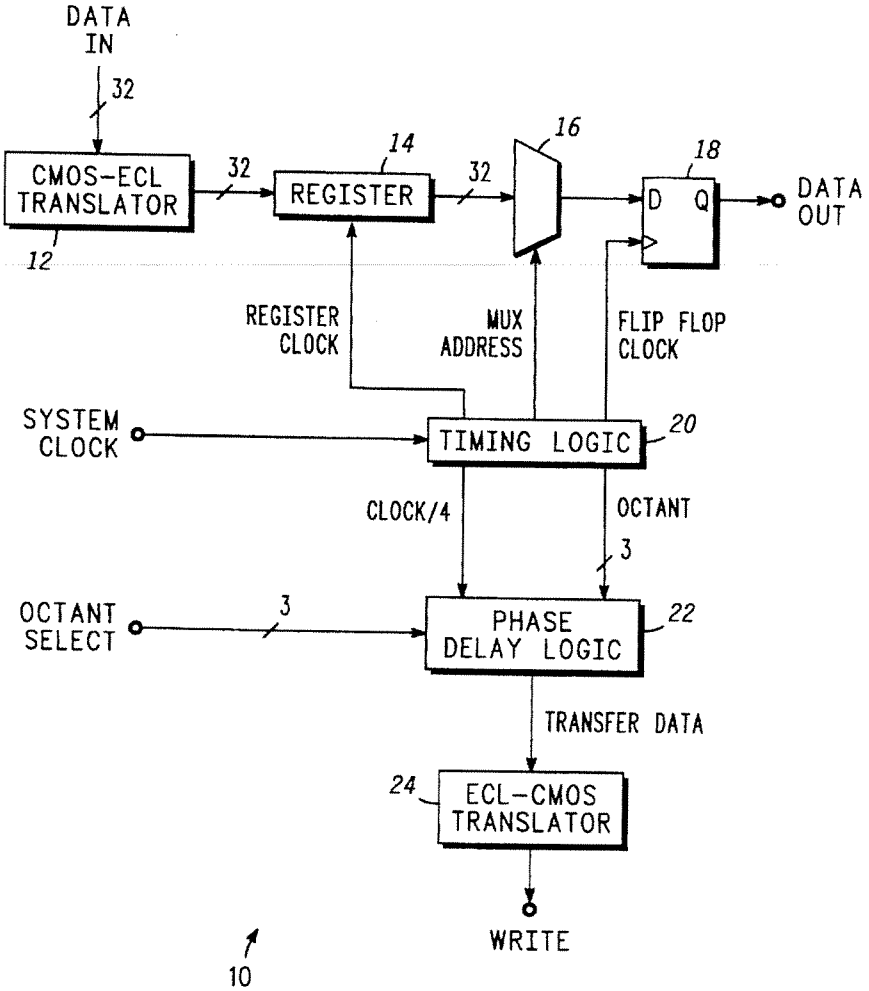
Primary Examiner—Marc S. Hoff

Attorney, Agent, or Firm—Robert D. Atkins

[57] **ABSTRACT**

A data conversion circuit receives input data from external sourcing logic and performs a parallel-serial conversion. Likewise, a data conversion circuit performs a serial-parallel conversion and presents output data to external sinking logic. In the parallel-serial conversion (**10**), the input data is translated (**12**) and stored in a register (**14**). A multiplexer (**16**) rotates through the data to provide the serial output. In the serial-parallel conversion (**70**), the input data is sequenced into a multiplexer (**74**) to achieve the parallel data word. The parallel data word is stored in a register (**76**) before presenting it to external logic. Phase delay logic (**22**) sets the delay of a transfer data control signal that requests data be read or written. Once the proper delay is determined by experimentation, the phase delay logic controls the phase of the transfer data control signal to request more data at the correct time, or present more data at the correct time, to allow maximum operating speed for the data converter.

19 Claims, 3 Drawing Sheets



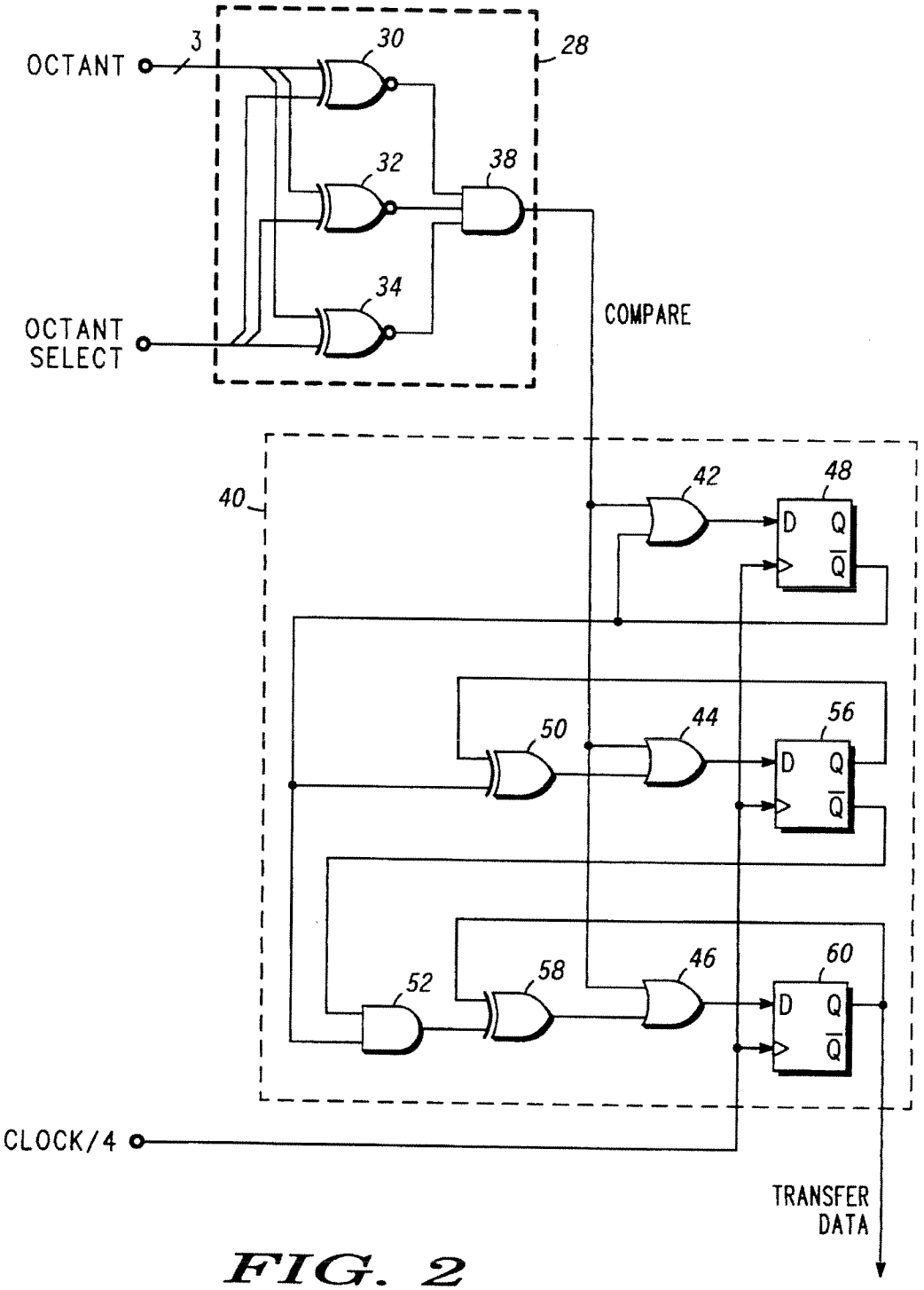

OCTANT
3
30
28
32
38
34
OCTANT SELECT
COMPARE
40
42
48
D
Q
Q
50
44
56
52
58
46
60
CLOCK/4
TRANSFER DATA

FIG. 2

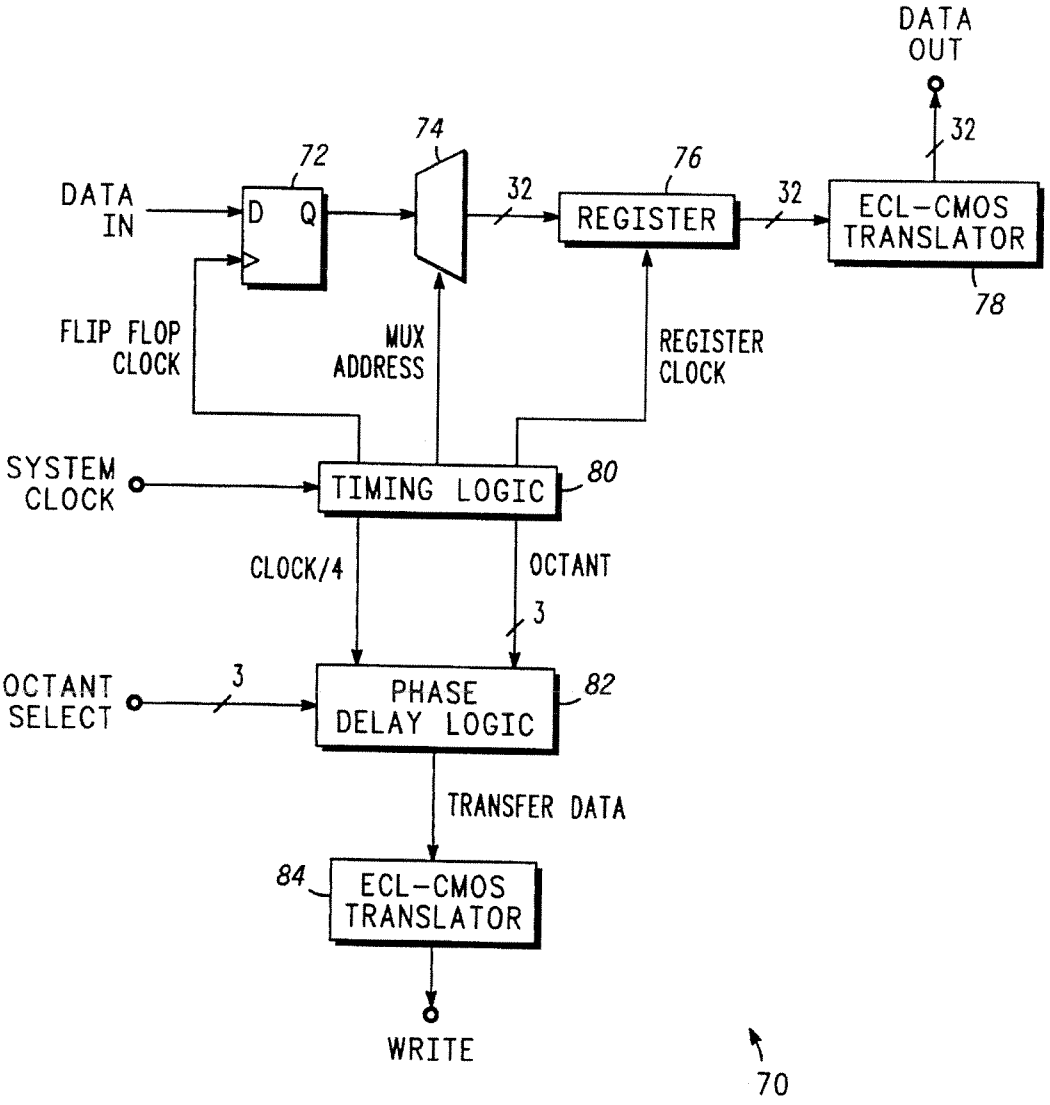

DATA OUT
32
74
72
76
DATA IN
D Q
32
REGISTER
32
ECL–CMOS TRANSLATOR
78
FLIP FLOP CLOCK
MUX ADDRESS
REGISTER CLOCK
SYSTEM CLOCK
TIMING LOGIC
80
CLOCK/4
OCTANT
3
OCTANT SELECT
3
PHASE DELAY LOGIC
82
TRANSFER DATA
84
ECL–CMOS TRANSLATOR
WRITE
70

FIG. 3

CIRCUIT AND METHOD OF TIMING DATA TRANSFERS

BACKGROUND OF THE INVENTION

The present invention relates in general to digital timing circuits and, more particularly, to controlling the phase of a data transfer signal to set the proper timing for reading or writing to a data register.

Parallel-serial converters are commonly used in digital circuit design to convert multi-bit signals to a string of data bits that are serially transmitted one at a time. Serial-parallel converters in turn convert the string of data bits back to multi-bit signals. In both applications, a data register is typically embedded within an integrated circuit that periodically receives new data sourced by external logic, or sources new data for external logic. Timing generation logic for reading or writing the data register is also embedded within the integrated circuit. The timing generation logic asserts a periodic signal to the external logic requesting data be presented to or removed from the data register.

Many applications involve high speed operation, say in the gigahertz range. The data transaction must be completed within a predetermined time period. That is, write data must be present and valid for a setup time before, and hold time after it is loaded into the register by a clock signal. Likewise, read data must be present and valid for a setup time before, and hold time after it is read by external logic. Unfortunately at such high data rates, the propagation delay uncertainties of the external logic are almost as long as the entire transaction period.

When the periodic signal is asserted to the external logic, requesting that new data be read or written, the external logic begins the time-consuming process of retrieving or storing new data. In the case of a request from the IC to the external logic to write new data, when the external logic finally presents new data to the integrated circuit, the new data typically propagates through buffer logic and eventually reaches the data register. The internal timing generation logic asserts a clock signal to load the data register. When the data transaction is so fast that propagation delay uncertainties consume almost the entire time period, there is no assurance that data arrives at the data register within register setup and hold-time constraints.

Since the write data register and timing logic are embedded within the integrated circuit, it is difficult to directly measure the actual write setup and hold-time. That is, the setup and hold-time are not readily observable by the external logic. If the write data setup and hold-time are unknown, the data rate of the external sourcing logic must be reduced to ensure sufficient setup and hold-time. Otherwise, where the propagation time uncertainty consumes a large portion of the transaction time period, the data transaction may fail to correctly time the data transfer under a worst-case timing analysis.

Hence, a need exists to properly set the timing of requesting more write data or read data for the data register to achieve maximum data transfer.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram illustrating a parallel-serial converter;

FIG. **2** is a schematic diagram illustrating the phase delay logic of FIG. **1**; and

FIG. **3** is a block diagram illustrating a serial-parallel converter.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to FIG. **1**, a parallel-serial converter **10** is shown suitable for manufacturing as an integrated circuit using conventional integrated circuit processes. A CMOS-ECL voltage translator circuit **12** receives a 32-bit DATA IN word from external sourcing logic (not shown) operating at CMOS logic levels. CMOS-ECL voltage translator circuit **12** provides a 32-bit signal operating at ECL logic levels to 32-bit register **14**. Register **14** loads data at rising edge of a REGISTER CLOCK signal. Multiplexer **16** rotates through the individual bit locations of register **14** under control of the MUX ADDRESS signal and provides serial bits to the data input of flipflop **18**. Flipflop **18** transfers the serial data signal to DATA OUT at its Q-output upon receiving a FLIPFLOP CLOCK signal.

Timing logic **20** operates in response to a SYSTEM CLOCK signal, running for example at 2.5 gigahertz, for providing the FLIPFLOP CLOCK signal and the REGISTER CLOCK signal. The FLIPFLOP CLOCK signal operates in phase and at the same frequency as the SYSTEM CLOCK. The REGISTER CLOCK signal is derived from dividing the SYSTEM CLOCK by value thirty-two. The REGISTER CLOCK signal is aligned on the same rising edge as the SYSTEM CLOCK. The MUX ADDRESS is reset to zero with each REGISTER CLOCK and counts up with the SYSTEM CLOCK to value thirty-two. Thus, the serialized data stream DATA OUT is sent at the SYSTEM CLOCK frequency with the duration of each serial bit time the same as the period of the SYSTEM CLOCK.

Timing logic **20** further provides a CLOCK/4 signal and a 3-bit OCTANT signal. The CLOCK/4 signal is derived by dividing the SYSTEM CLOCK by value four with alignment on the rising edges of SYSTEM CLOCK. The OCTANT signal takes one of eight binary encoded values (0 through 7) as seen in Table 1. During a first group of four consecutive SYSTEM CLOCKS **C0–C3**, OCTANT has a value "000". During the second group of four consecutive SYSTEM CLOCKS C4–C7, OCTANT has a value "001", and so on. The OCTANT signal changes state at each rising edge of CLOCK/4, for example, by incrementing a counter (not shown). Timing logic **20** includes combinational logic to divide the SYSTEM CLOCK and reset the MUX ADDRESS signal. Such combinational logic can be implemented from the aforedescribed operations.

TABLE 1

SYSTEM CLOCK	OCTANT
C0–C3	"000"
C4–C7	"001"
C8–C11	"010"
C12–C15	"011"
C16–C19	"100"
C20–C23	"101"
C24–C27	"110"
C28–C31	"111"

Phase delay logic circuit **22** receives CLOCK/4 and OCTANT signals from timing logic **20**, and an OCTANT SELECT signal from the external logic (not shown). ECL-CMOS translator **24** converts the TRANSFER DATA signal from phase delay logic circuit **22** to CMOS logic levels for the external logic. Upon receiving the WRITE control

signal, the external logic sends the next 32-bit DATA IN word.

It is important for the overall circuit operation that the output signal from REGISTER **14** does not become metastable. The 32-bit data at the output of translator circuit **12** must be stable for a finite "setup time" before the rising edge of REGISTER CLOCK. Likewise, the 32-bit data must remain stable for a finite "hold-time" after the rising edge of REGISTER CLOCK to ensure that register **14** clocks in valid data. Any violation of setup and hold-time may cause the register output to become metastable, yielding indeterminate logic levels for an indeterminate time duration.

Accordingly, as a feature of the present invention, phase delay logic circuit **22** sets the timing of TRANSFER DATA signal by altering its phase as programmed by the 3-bit OCTANT SELECT signal to request more data at the proper time to allow parallel-serial converter **10** to complete processing the previous data. In practice during a calibration sequence, the OCTANT SELECT signal may be set to various values to determine proper delay time necessary before the WRITE is asserted so that the next DATA IN word arrives at the optimum time to ensure proper data set-up and hold times at the input of register **14** and to allow time to complete processing the previous data. Once the proper delay is determined by experimentation, phase delay logic circuit **22** asserts the TRANSFER DATA signal at the correct time by controlling its phase to allow maximum operating speed for parallel-serial converter **10** given the required set-up and hold-time of register **14**.

Turning to FIG. **2**, further detail of phase delay logic circuit **22** is shown including a digital comparator **28** implemented as exclusive-NOR (XNOR) gates **30**, **32** and **34** and AND gate **38**. XNOR gate **30** receives bit**0** of the OCTANT signal and bit**0** of the OCTANT SELECT signal. XNOR gate **32** receives bit**1** of the OCTANT signal and bit**1** of the OCTANT SELECT signal. XNOR gate **34** receives bit**2** of the OCTANT signal and bit**2** of the OCTANT SELECT signal. The outputs of XNOR gates **32–36** are coupled to inputs of AND gate **38**. If the OCTANT signal matches the OCTANT SELECT signal, AND gate **38** receives all logic ones and provides a logic one COMPARE signal. Otherwise, the COMPARE signal from AND gate **38** is logic zero.

Logic block **40** provides a symmetric 50% duty cycle for the TRANSFER DATA signal by counting down after the COMPARE signal sets the TRANSFER DATA (most significant bit of three bit down-counter) to logic one. The COMPARE signal from AND gate **38** is applied to first inputs of OR gates **42**, **44** and **46**. The output of OR gate **42** is coupled to the D-input of flipflop **48**. The $\overline{Q}$-output of flipflop **48** is coupled to the second input of OR gate **42**, to an input of exclusive-OR (XOR) gate **50**, and to an input of AND gate **52**. The output of XOR gate **50** is coupled to a second input of OR gate **44** that in turn has an output coupled to the D-input of flipflop **56**. The Q-output of flipflop **56** is coupled to the second input of XOR gate **50**, while the $\overline{Q}$-output of flipflop **56** is coupled to the second input of AND gate **52**. The output of AND gate **52** is coupled to a first input of XOR gate **58** that in turn has an output coupled to the second input of OR gate **46**. The output of OR gate **46** is coupled to the D-input of flipflop **60**. The Q-output of flipflop **60** is coupled to the second input of XOR gate **58** and further provides the TRANSFER DATA signal to ECL-CMOS translator **24** in FIG. **1**. Flipflops **48**, **56** and **60** receive the CLOCK/4 signal at their clock inputs.

During the 32-bit parallel to serial conversion, the 3-bit OCTANT signal increments on every rising edge of CLOCK/4, i.e. every four SYSTEM CLOCKS. When the 3-bit OCTANT signal matches the externally-supplied 3-bit OCTANT SELECT signal, the COMPARE signal is asserted as logic one. The Q-outputs of flipflops **48**, **56** and **60** go to logic one on the next rising edge of the CLOCK/4 signal. The TRANSFER DATA signal goes to logic one. When the OCTANT signal increments to its next value and COMPARE returns to logic zero, flipflops **48**, **56** and **60** operate as a 3-bit synchronous down counter and decrement with each rising edge of CLOCK/4. Since the TRANSFER DATA signal is the most significant bit of the down counter, it remains logic one for the first half of the counts and returns to logic zero for the second half of the counts. Logic block **40** thus provides a symmetric 50% duty cycle for the TRANSFER DATA signal.

For example, assume that the 32-bit DATA IN signal is latched into register **14** by the REGISTER CLOCK. In the present example, it has been determined by experimentation that the OCTANT SELECT signal "001" sets the proper phase delay before asserting TRANSFER DATA to the external logic to send the next DATA IN word. The delay determines the amount of time parallel-serial converter **10** needs to complete processing the present data word and be ready for the next. Assume that the Q-outputs of the flipflops begin at logic one and the $\overline{Q}$-outputs begin as logic zero. The first four SYSTEM CLOCKS C**0**–C**3** correspond to multiplexer **16** reading the four least significant bits D**0**–D**3** from register **14**. At the first rising edge of CLOCK/4 (clock C**0**), the OCTANT signal is "**000**" and does not match the OCTANT SELECT signal "001". Consequently, the COMPARE signal is logic zero.

At the second rising edge of CLOCK/4 (clock C**4**), the OCTANT signal switches to "001" and matches the OCTANT SELECT signal causing the COMPARE signal goes to logic one. The outputs of OR gates **42–46** go to logic one due to the logic one COMPARE signal for the initial state of the down count. Four SYSTEM CLOCKS later, the third rising edge of CLOCK/4 (clock C**8**) clocks the logic ones into flipflops **48**, **56** and **60** and sets their Q-outputs to logic one. The OCTANT signal switches to "010" and no longer matches the OCTANT SELECT signal. The COMPARE signal returns to logic zero. XOR gate **50** receives a logic zero from the $\overline{Q}$-output of flipflop **48** and a logic one from the Q-output of flipflop **56** and sets the second input of OR gate **44** to logic one. The D-input of flipflop **56** receives a logic one from OR gate **44**. AND gate **52** receives logic zeroes from flipflops **48** and **56**. XOR gate **58** receives a logic zero from AND gate **52** and a logic one from flipflop **60** and provides a logic one to OR gate **46**. The D-input of flipflop **60** goes to logic one.

The fourth rising edge of CLOCK/4 (clock C**12**) sets the $\overline{Q}$-output of flipflop **48** to logic one while the Q-outputs of flipflops **56** and **60** remain logic one. The output of OR gate **42** goes to logic one. XOR gate **50** receives a logic one from the $\overline{Q}$-output of flipflop **48** and a logic one from the Q-output of flipflop **56** and sets the second input of OR gate **44** to logic zero. The D-input of flipflop **56** receives a logic zero from OR gate **44**. AND gate **52** receives a logic one from flipflop **48** and a logic zero from flipflop **56**. XOR gate **58** receives a logic zero from AND gate **52** and a logic one from flipflop **60** and provides a logic one to OR gate **46**. The D-input of flipflop **60** goes to logic one.

The fifth rising edge of CLOCK/4 (clock C**16**) sets the Q-outputs of flipflops **48** and **60** to logic one while the Q-output of flipflop **56** goes to logic zero. The output of OR gate **42** goes to logic zero. XOR gate **50** receives logic zeroes from the $\overline{Q}$-output of flipflop **48** and the Q-output of

flipflop **56** and sets the second input of OR gate **44** to logic zero. The D-input of flipflop **56** receives a logic zero from OR gate **44**. AND gate **52** receives a logic zero from flipflop **48** and a logic one from flipflop **56**. XOR gate **58** receives a logic zero from AND gate **52** and a logic one from flipflop **60** and provides a logic one to OR gate **46**. The D-input of flipflop **60** goes to logic one.

The sixth rising edge of CLOCK/4 (clock C**20**) sets the $\overline{Q}$-outputs of flipflops **48** and **56** to logic one while the Q-output of flipflop **60** remains logic one. XOR gate **50** receives a logic one from the $\overline{Q}$-output of flipflop **48** and a logic zero from the Q-output of flipflop **56** and sets the second input of OR gate **44** to logic one. The D-input of flipflop **56** receives a logic one from OR gate **44**. AND gate **52** receives logic ones from flipflops **48** and flipflop **56**. XOR gate **58** receives a logic one from AND gate **52** and a logic one from flipflop **60** and provides a logic zero to OR gate **46**. The D-input of flipflop **60** goes to logic zero.

The seventh rising edge of CLOCK/4 (clock C**24**) sets the TRANSFER DATA signal to logic zero. The TRANSFER DATA signal remains logic zero for the next four CLOCK/4 cycles, i.e. C**24**–C**31** and C**0**–C**7**, as the down counter completes the second half of its count down sequence. Logic **40** thus provides a symmetric 50% duty cycle. Either edge of the TRANSFER DATA signal may be used to trigger the external logic to send more data to parallel-serial converter **10**. By controlling the phase of TRANSFER DATA, the correct timing is established for data transfer so that the requested data arrives at the optimum time to maximize the operating speed of parallel-serial converter **10**.

The aforedescribed phase control over the TRANSFER DATA is equally applicable to serial-parallel conversion such as shown in FIG. **3**. Serial-parallel converter **70** is shown suitable for manufacturing as an integrated circuit using conventional integrated circuit processes. The data input of flipflop **72** receives the serial DATA IN signal from external sourcing logic (not shown) and passes it to multiplexer **74** at each FLIPFLOP CLOCK. Multiplexer **74** rotates through its individual bit locations under control of the MUX ADDRESS signal and provides parallel bits to register **76**. Register **76** loads data at rising edge of a REGISTER CLOCK signal. A CMOS-ECL voltage translator circuit **78** converts the 32-bit data word from register **76** to CMOS logic levels.

Timing logic **80** operates in response to a SYSTEM CLOCK signal, operating for example at 2.5 gigahertz, for providing the FLIPFLOP CLOCK signal and the REGISTER CLOCK signal. The FLIPFLOP CLOCK signal operates in phase and at the same frequency as the SYSTEM CLOCK. The REGISTER CLOCK signal are derived from dividing the SYSTEM CLOCK by value thirty-two. The REGISTER CLOCK signal is aligned on the same rising edge as the SYSTEM CLOCK. The MUX ADDRESS is reset to zero with each REGISTER CLOCK and counts up with the SYSTEM CLOCK to value thirty-two. Thus, the serialized data stream DATA OUT is sent at the SYSTEM CLOCK frequency with the duration of each serial bit time the same as the period of the SYSTEM CLOCK. Timing logic **20** further provides a CLOCK/4 signal and a 3-bit OCTANT signal. The CLOCK/4 signal is derived by dividing the SYSTEM CLOCK by value four aligned with the rising edges of SYSTEM CLOCK. The OCTANT signal takes one of eight binary encoded values (0 through 7) as seen in Table 1. Timing logic **80** includes combinational logic to divide the SYSTEM CLOCK and reset the MUX ADDRESS signal. Such combinational logic can be implemented from the aforedescribed operations.

Phase delay logic circuit **82** receives CLOCK/4 and OCTANT signals from timing logic **80**, and an OCTANT SELECT signal from external logic (not shown). ECL-CMOS translator **84** converts the TRANSFER DATA signal from phase delay logic circuit **82** to CMOS logic levels for the external logic. Upon receiving the WRITE control signal, the external logic sends the next DATA IN bit. Phase delay logic circuit **82** follows the same description given in FIG. **2** and asserts the TRANSFER DATA signal at the correct time to allow maximum operating speed for serial-parallel converter **70** given the required set-up and hold-time of register **76**.

By now it should be appreciated that the present invention provides proper timing of the data transfer between external data sourcing or sinking logic and data conversion circuits. Phase delay logic sets the delay for a transfer data control signal as programmed by a select signal. During a calibration sequence, the select signal is set to various values to determine proper delay time necessary before requesting that more data be read or written. Once the proper delay is determined by experimentation, the phase delay logic circuit asserts the transfer data signal at the correct time by controlling its phase, to allow maximum operating speed for the data conversion given the required set-up and hold-time of the embedded register and of the external logic. By controlling the phase of transfer data requests, the correct timing is established to ensure proper data set-up and hold times and to allow complete processing before the next data word needs to be read or written.

While specific embodiments of the present invention have been shown and described, further modifications and improvements will occur to those skilled in the art. It is understood that the invention is not limited to the particular forms shown and it is intended for the appended claims to cover all modifications which do not depart from the spirit and scope of this invention. The present invention is applicable to other types of data processing circuits that must control timing of incoming data.

What is claimed is:

1. A phase delay circuit, comprising:

a comparator having first and second inputs and an output, said first input receiving a first control signal, said second input receiving a second control signal, said output providing a compare signal having a first state when said first and second control signals match; and

a down counter responsive to said compare signal for initializing a count value and responsive to a clock signal for counting down to generate an output signal having a symmetric duty cycle.

2. The circuit of claim **1** wherein said down counter includes:

a first OR gate having first and second inputs and an output, said first input being coupled for receiving said compare signal; and

a first flipflop having a data input, a clock input, and an inverted output, said data input being coupled to said output of said first OR gate, said inverted output being coupled to said second input of said first OR gate, said clock input being coupled for receiving said clock signal.

3. The circuit of claim **2** wherein said down counter further includes:

a first exclusive-OR gate having first and second inputs and an output, said first input being coupled to said inverted output of said first flipflop;

a second OR gate having first and second inputs and an output, said first input being coupled for receiving said

compare signal, said second input being coupled to said output of said first exclusive-OR gate; and

a second flipflop having a data input, a clock input, and first and second complementary outputs, said data input being coupled to said output of said second OR gate, said first complementary output being coupled to said second input of said first exclusive-OR gate, said clock input being coupled for receiving said clock signal.

4. The circuit of claim **3** wherein said down counter further includes:

a first AND gate having first and second inputs and an output, said first input being coupled to said inverted output of said first flipflop, said second input being coupled to said second complementary output of said second flipflop;

a second exclusive-OR gate having first and second inputs and an output, said first input being coupled to said output of said first AND gate;

a third OR gate having first and second inputs and an output, said first input being coupled for receiving said compare signal, said second input being coupled to said output of said second exclusive-OR gate; and

a third flipflop having a data input, a clock input, and an output, said data input being coupled to said output of said third OR gate, said output being coupled to said second input of said second exclusive-OR gate and providing said output signal of said down counter, said clock input being coupled for receiving said clock signal.

5. The circuit of claim **4** wherein said comparator includes:

a third exclusive-OR gate having first and second inputs and an output, said first input being coupled for receiving a first bit of said first control signal, said second input being coupled for receiving a first bit of said second control signal;

a fourth exclusive-OR gate having first and second inputs and an output, said first input being coupled for receiving a second bit of said first control signal, said second input being coupled for receiving a second bit of said second control signal; and

a second AND gate having first and second inputs and an output, said first input being coupled to said output of said third exclusive-OR gate, said second input being coupled to said output of said fourth exclusive-OR gate, said output providing said compare signal.

6. The circuit of claim **5** wherein said comparator further includes a fifth exclusive-OR gate having first and second inputs and an output, said first input being coupled for receiving a third bit of said first control signal, said second input being coupled for receiving a third bit of said second control signal, said output being coupled to a third input of said second AND gate.

7. A method of selecting phase delay of a transfer data control signal, comprising the steps of:

comparing first and second control signals and generating a compare signal having a first state when said first and second control signals match; and

initializing a count value in response to said compare signal; and

counting down said count value in response to a clock signal to provide a most significant bit of said count value with a symmetric duty cycle.

8. A data conversion circuit, comprising:

a register having an input coupled for receiving parallel input data and having an output;

a multiplexer having an input coupled to said output of said register for providing serial data;

a comparator having first and second inputs and an output, said first input receiving a first control signal, said second input receiving a second control signal, said output providing a compare signal having a first state when said first and second control signals match; and

a down counter responsive to said compare signal for initializing a count value and responsive to a clock signal for counting down to generate a transfer data signal having a symmetric duty cycle to enable transfer of said parallel input data to said register.

9. The circuit of claim **8** wherein said down counter includes:

a first OR gate having first and second inputs and an output, said first input being coupled for receiving said compare signal; and

a first flipflop having a data input, a clock input, and an inverted output, said data input being coupled to said output of said first OR gate, said inverted output being coupled to said second input of said first OR gate, said clock input being coupled for receiving said clock signal.

10. The circuit of claim **9** wherein said down counter further includes:

a first exclusive-OR gate having first and second inputs and an output, said first input being coupled to said inverted output of said first flipflop;

a second OR gate having first and second inputs and an output, said first input being coupled for receiving said compare signal, said second input being coupled to said output of said first exclusive-OR gate; and

a second flipflop having a data input, a clock input, and first and second complementary outputs, said data input being coupled to said output of said second OR gate, said first complementary output being coupled to said second input of said first exclusive-OR gate, said clock input being coupled for receiving said clock signal.

11. The circuit of claim **10** wherein said down counter further includes:

a first AND gate having first and second inputs and an output, said first input being coupled to said inverted output of said first flipflop, said second input being coupled to said second complementary output of said second flipflop;

a second exclusive-OR gate having first and second inputs and an output, said first input being coupled to said output of said first AND gate;

a third OR gate having first and second inputs and an output, said first input being coupled for receiving said compare signal, said second input being coupled to said output of said second exclusive-OR gate; and

a third flipflop having a data input, a clock input, and an output, said data input being coupled to said output of said third OR gate, said output being coupled to said second input of said second exclusive-OR gate and providing said output signal of said down counter, said clock input being coupled for receiving said clock signal.

12. The circuit of claim **11** wherein said comparator includes:

a third exclusive-OR gate having first and second inputs and an output, said first input being coupled for receiving a first bit of said first control signal, said second input being coupled for receiving a first bit of said second control signal;

a fourth exclusive-OR gate having first and second inputs and an output, said first input being coupled for receiving a second bit of said first control signal, said second input being coupled for receiving a second bit of said second control signal; and

a second AND gate having first and second inputs and an output, said first input being coupled to said output of said third exclusive-OR gate, said second input being coupled to said output of said fourth exclusive-OR gate, said output providing said compare signal.

13. The circuit of claim **12** wherein said comparator further includes a fifth exclusive-OR gate having first and second inputs and an output, said first input being coupled for receiving a third bit of said first control signal, said second input being coupled for receiving a third bit of said second control signal, said output being coupled to a third input of said second AND gate.

14. A data conversion circuit, comprising:

a multiplexer having an input coupled for receiving serial input data and having an output;

a register having an input coupled to said output of said register for providing prarllel data;

a comparator having first and second inputs and an output, said first input receiving a first control signal, said second input receiving a second control signal, said output providing a compare signal having a first state when said first and second control signals match; and

a down counter responsive to said compare signal for initializing a count value and responsive to a clock signal having a symmetric duty cycle to enable transfer of said serial input data to said register.

15. The circuit of claim **14** wherein said down counter includes:

a first OR gate having first and second inputs and an output, said first input being coupled for receiving said compare signal; and

a first flipflop having a data input, a clock input, and an inverted output, said data input being coupled to said output of said first OR gate, said inverted output being coupled to said second input of said first OR gate, said clock input being coupled for receiving said clock signal.

16. The circuit of claim **15** wherein said down counter further includes:

a first exclusive-OR gate having first and second inputs and an output, said first input being coupled to said inverted output of said first flipflop;

a second OR gate having first and second inputs and an output, said first input being coupled for receiving said compare signal, said second input being coupled to said output of said first exclusive-OR gate; and

a second flipflop having a data input, a clock input, and first and second complementary outputs, said data input being coupled to said output of said second OR gate, said first complementary output being coupled to said second input of said first exclusive-OR gate, said clock input being coupled for receiving said clock signal.

17. The circuit of claim **161**wherein said down counter further includes:

a first AND gate having first and second inputs and an output, said first input being coupled to said inverted output of said first flipflop, said second input being coupled to said second complementary output of said second flipflop;

a second exclusive-OR gate having first and second inputs and an output, said first input being coupled to said output of said first AND gate;

a third OR gate having first and second inputs and an output, said first input being coupled for receiving said compare signal, said second input being coupled to said output of said second exclusive-OR gate; and

a third flipflop having a data input, a clock input, and an output, said data input being coupled to said output of said third OR gate, said output being coupled to said second input of said second exclusive-OR gate and providing said output signal of said down counter, said clock input being coupled for receiving said clock signal.

18. The circuit of claim **17** wherein said comparator includes:

a third exclusive-OR gate having first and second inputs and an output, said first input being coupled for receiving a first bit of said first control signal, said second input being coupled for receiving a first bit of said second control signal;

a fourth exclusive-OR gate having first and second inputs and an output, said first input being coupled for receiving a second bit of said first control signal, said second input being coupled for receiving a second bit of said second control signal; and

a second AND gate having first and second inputs and an output, said first input being coupled to said output of said third exclusive-OR gate, said second input being coupled to said output of said fourth exclusive-OR gate, said output providing said compare signal.

19. The circuit of claim **18** wherein said comparator further includes a fifth exclusive-OR gate having first and second inputs and an output, said first input being coupled for receiving a third bit of said first control signal, said second input being coupled for receiving a third bit of said second control signal, said output being coupled to a third input of said second AND gate.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 5,563,594
DATED : October 8, 1996
INVENTOR(S) : David K. Ford et al.

It is certified that error appears in the above-indentified patent and that said Letters Patent is hereby corrected as shown below:

In claim 14, column 9, line 30, insert --for counting down to generate a transfer data signal-- after "signal".

In claim 17, column 10, line 7, delete "161wherein" and insert --16 wherein--.

Signed and Sealed this

Twenty-ninth Day of April, 1997

Attest:

Attesting Officer

BRUCE LEHMAN

Commissioner of Patents and Trademarks

[redacted]

EXHIBIT B

US006362644B1

(12) **United States Patent**
Jeffery et al.

(10) **Patent No.: US 6,362,644 B1**
(45) **Date of Patent: Mar. 26, 2002**

(54) **PROGRAMMABLE TERMINATION FOR INTEGRATED CIRCUITS**

(75) Inventors: **Philip A. Jeffery**, Tempe; **Stephen G. Shook**, Gilbert, both of AZ (US)

(73) Assignee: **Semiconductor Components Industries LLC**, Phoenix, AZ (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/630,090**

(22) Filed: **Aug. 1, 2000**

(51) **Int. Cl.**[7] **H03K 17/16**
(52) **U.S. Cl.** **326/30**; 326/101
(58) **Field of Search** 326/30, 62, 63, 326/101; 327/333, 564, 565

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,341,039 A * 8/1994 Fukumoto 326/30
5,374,861 A * 12/1994 Kubista 326/30
5,731,711 A * 3/1998 Gabara 326/30
5,781,028 A * 7/1998 Decuir 326/30
6,114,898 A * 9/2000 Okayasu 327/437

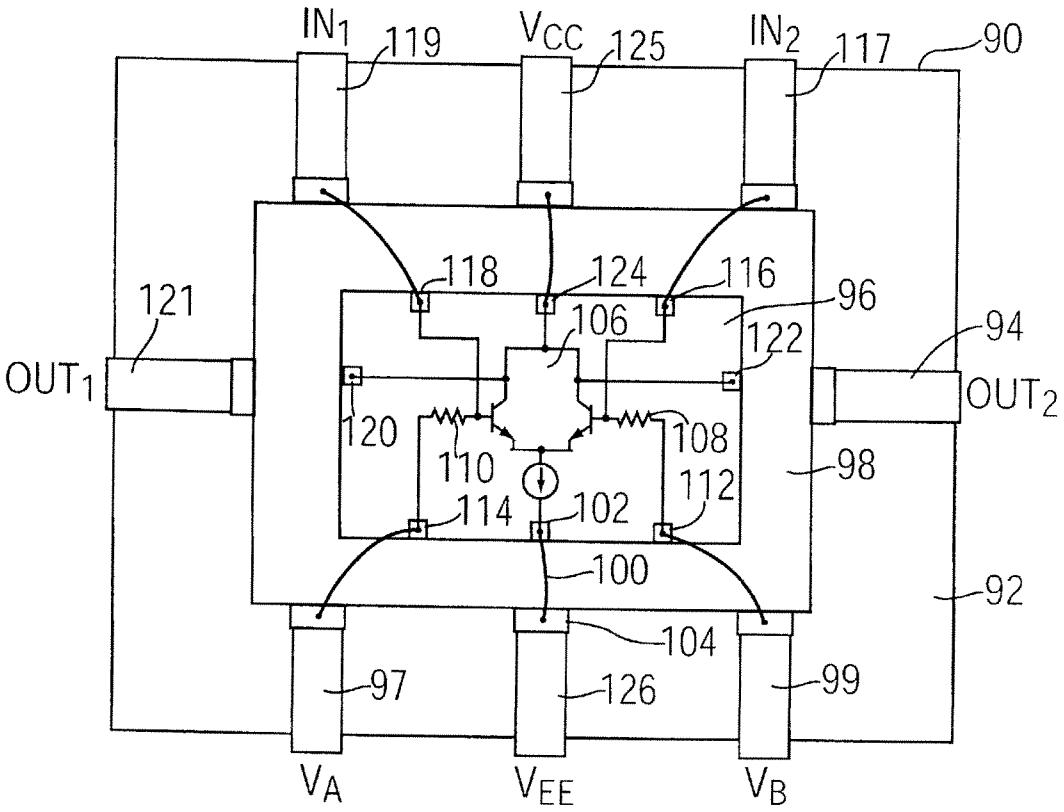
* cited by examiner

Primary Examiner—Tuan T. Lam

(57) **ABSTRACT**

A receiver circuit **(16)** is programmable to operate with different logic family driver circuits **(10)**. The receiver circuit has two external configuration pins **(22,) 24)** that are configured to provide the necessary termination for the type of logic family driver circuit used. To terminate the receiver circuit **(16)** for an ECL application will require first and second configuration pins **(22,24)** are connected to V_{CC}—2 volts. To terminate the receiver circuit **(16)** for a CML application will require the first configuration pin **(22)** and the second configuration pin **(24)** are connected to V_{CC}. LVDS termination for the receiver circuit **(16)** requires the first configuration pin **(22)** and the second configuration pin **(24)** are connected together. The configuration pins are external to a semiconductor package **(14)** housing the receiver circuit.

16 Claims, 3 Drawing Sheets



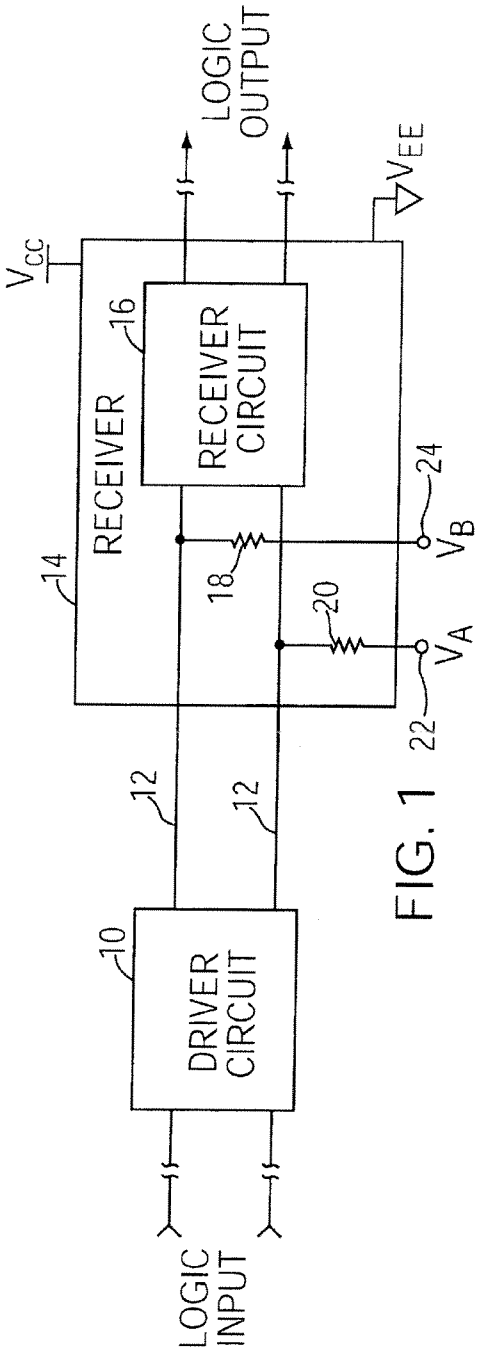

LOGIC OUTPUT
V_{EE}
V_{CC}
RECEIVER
16
RECEIVER CIRCUIT
14
18
20
24
V_B
V_A
22
12
12
10
DRIVER CIRCUIT
LOGIC INPUT

FIG. 1

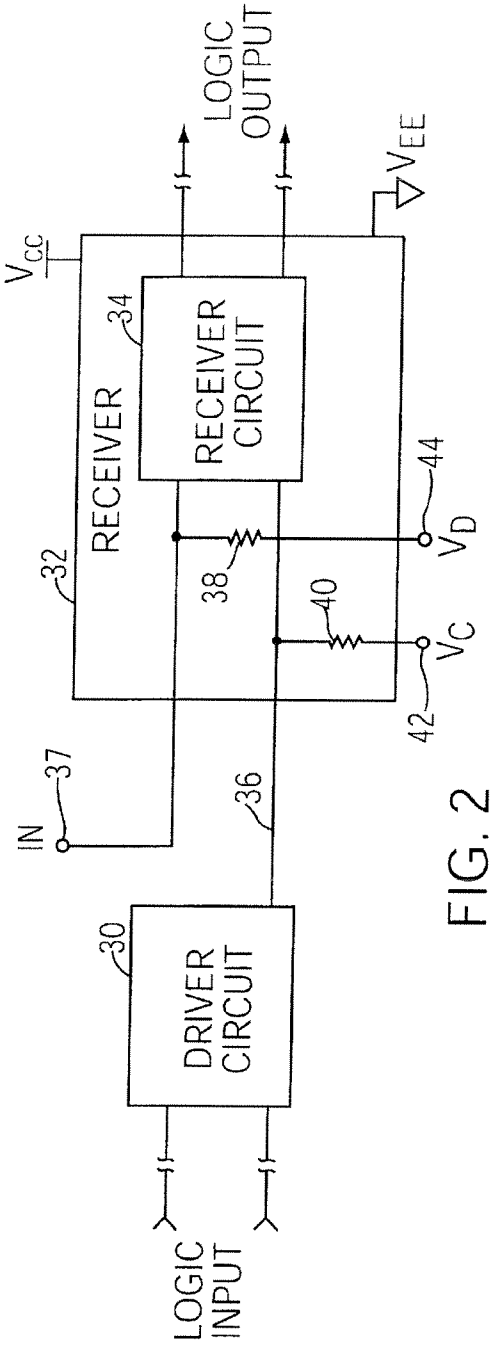

LOGIC OUTPUT
V_{EE}
V_{CC}
RECEIVER
34
RECEIVER CIRCUIT
32
38
40
44
V_D
V_C
42
IN
37
36
30
DRIVER CIRCUIT
LOGIC INPUT

FIG. 2

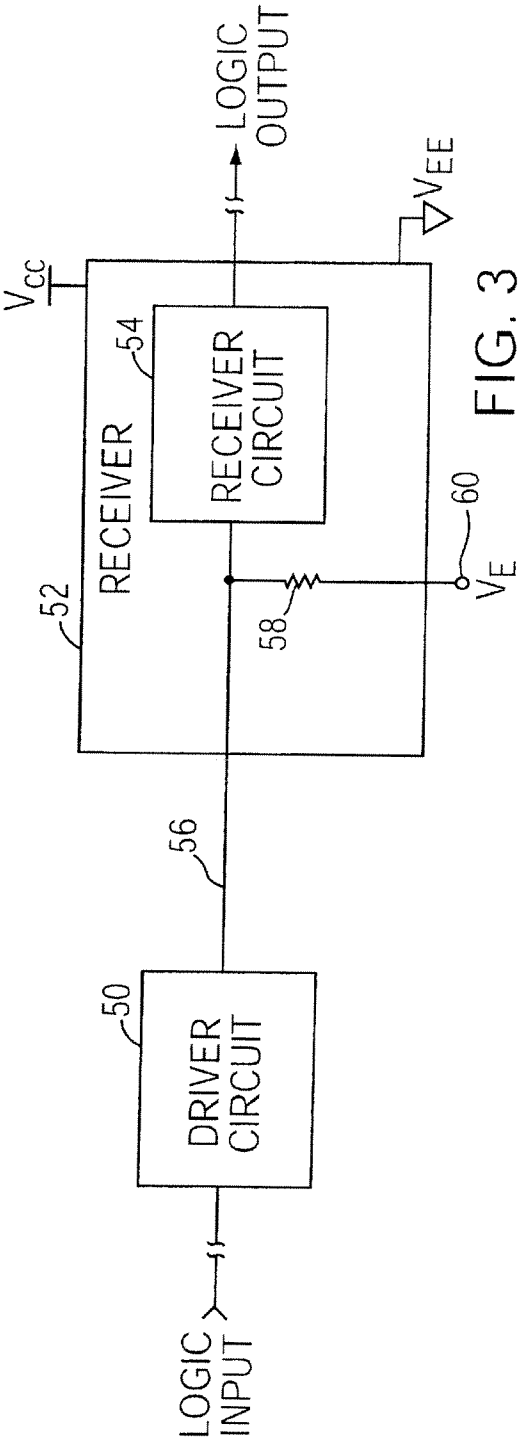

LOGIC OUTPUT
V_{EE}
V_{CC}
54
RECEIVER CIRCUIT
RECEIVER
52
60
V_E
58
56
50
DRIVER CIRCUIT
LOGIC INPUT

FIG. 3

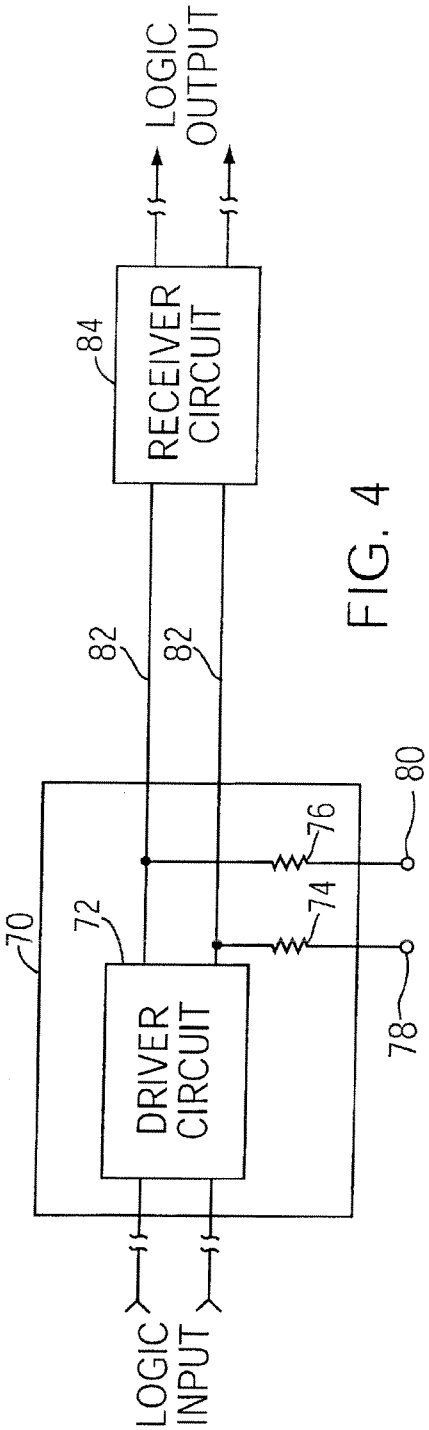

LOGIC OUTPUT
84
RECEIVER CIRCUIT
82
82
80
76
74
70
72
DRIVER CIRCUIT
78
LOGIC INPUT

FIG. 4

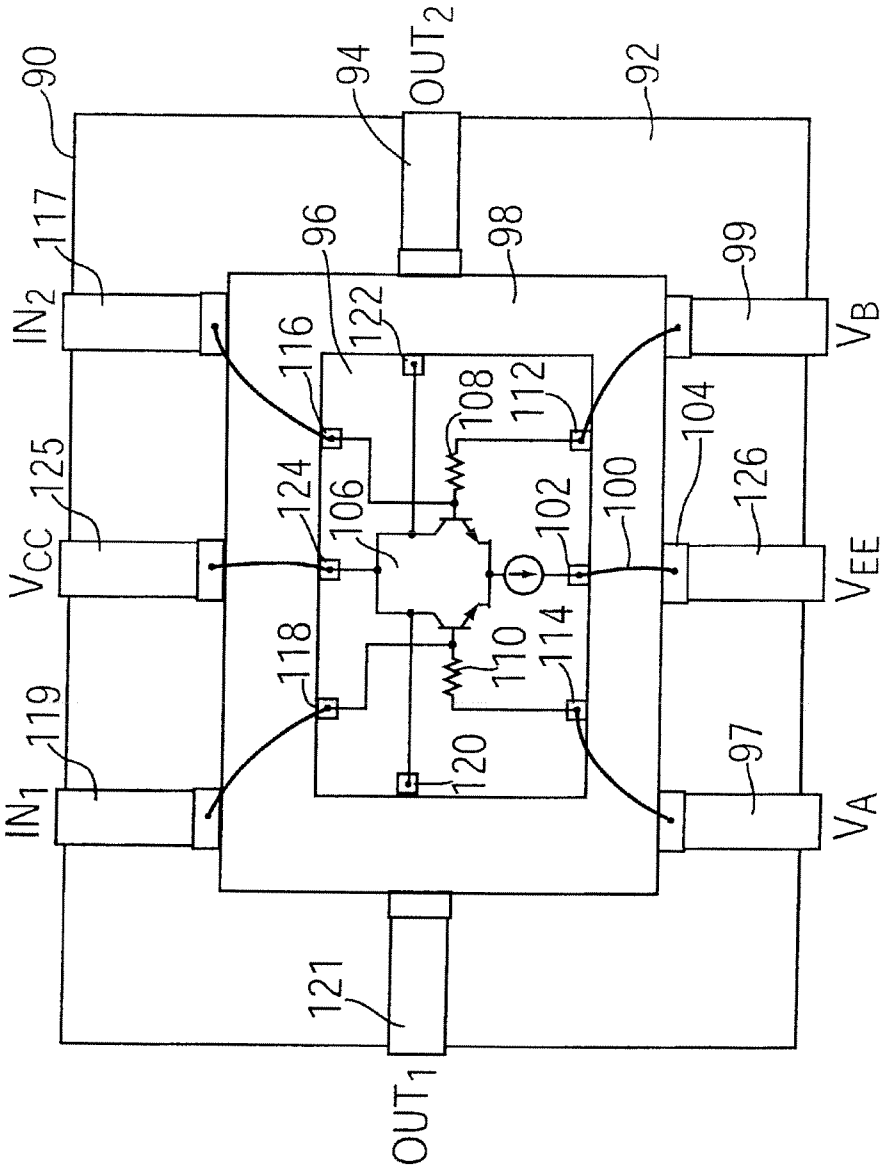

90
94
OUT2
92
117
96
98
99
IN2
VB
116
122
108
112
104
125
124
106
102
100
126
VCC
VEE
118
110
114
119
120
97
IN1
VA
121
OUT1

FIG. 5

PROGRAMMABLE TERMINATION FOR INTEGRATED CIRCUITS

BACKGROUND OF THE INVENTION

The present invention relates in general to electronic circuits and, more particularly, to logic circuits.

Many logic family applications have logic devices that operate within a mixed signal environment. The logic devices have logic drivers that may communicate with a logic receiver of a different logic family type. Typically, different logic family devices communicate with each other using translators to convert, for example, an ECL signal from the logic driver to a CMOS signal received at the logic receiver. A different type of translator is required for each type of logic driver and logic receiver used within the mixed signal environment. In addition, systems usually have an external termination scheme on an interconnect transmission line between the logic driver and logic receiver so the logic receiver circuit is terminated to receive the specific logic driver family type. The termination is a resistance that provides a termination for the logic device through to a voltage source Vtt. The voltage source Vtt is typically different for each logic family application. The resistance is typically chosen to equal the impedance of the interconnect transmission line to help reduce interconnect signal distortion. It is more of an advantage to have terminations as close as possible to the logic receiver circuit to help reduce interconnect signal distortion even more. Also, prior art termination schemes typically require different termination connections are used for each type of logic family device. For example, to use an ECL logic device requires a 50 ohm termination to a Vtt voltage source. A CML logic device may require termination through a resistance to a different voltage source. Most prior art logic family devices also have the termination resistors hard-wired to a circuit board making it difficult to change terminations for different logic family applications.

Hence, it is desired to have a logic receiver circuit that is programmable to allow the logic receiver circuit to communicate with different logic family driver circuits. Furthermore, it is desirable to have the terminations internal to the logic receiver circuit package so the terminations are close to the receiving circuit to help eliminate transmitted signal noise. The invention disclosed herein will address the above problems.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a schematic diagram of a driver and receiver circuit in a differential configuration;

FIG. **2** is a schematic diagram of a driver and receiver circuit in a single-ended configuration;

FIG. **3** is a schematic diagram of a driver and receiver circuit in a modified single-ended configuration;

FIG. **4** is a schematic diagram of a driver and receiver circuit in a differential configuration with driver circuit terminations; and

FIG. **5** is a schematic diagram of a receiver circuit showing semiconductor and package connections.

DETAILED DESCRIPTION OF THE PREFERED EMBODIMENT

FIG. **1** illustrates an embodiment of a driver circuit and a receiver circuit system used in a differential configuration. The differential configuration receives a logic input signal at driver circuit **10**. Driver circuit **10** is a device from a typical

logic family, e.g. ECL, CML, LVDS, CMOS, and TTL, or can be an analog driver circuit. The primary purpose of driver circuit **10** is to provide a signal boost for the logic input signal. At the output to driver circuit **10** is differential line **12** which transmits a differential signal from driver circuit **10** to receiver package **14**. Receiver package **14** is a semiconductor package housing receiver circuit **16**. V_{CC} and V_{EE} are power supply potentials to receiver package **14** providing power to receiver circuit **16**. Receiver circuit **16** receives a differential input signal on differential line **12** and provides a logic output signal. Receiver circuit **16** is typically a differential receiver circuit amplifier manufactured as a semiconductor die. Receiver circuit **16** and receiver package **14** are an integrated receiver circuit.

Differential line **12** is terminated with load element **18** and load element **20**. Load element **18** is connected to configuration pin **24** and load element **20** is connected to configuration pin **22**. Load elements **18, 20** are resistors contained within receiver package **14** having a resistance of 50, 75, or 100 ohms. Configuration pins **22, 24** are external pins connected to receiver package **14** and are programmable so receiver circuit **16** can communicate with different logic family drivers. To program configuration pins **22, 24**, the pins are terminated using a configuration which is dependent on the desired logic family application. The configuration of receiver circuit **16** is controlled by connecting configuration pin **22** (V_A) and configuration pin **24** (V_B) as follows.

ECL:	$V_A = V_B = V_{cc} - 2$ volts
CML:	$V_A = V_B = V_{CC}$
LVDS:	V_A connected to V_B

For example, to terminate receiver circuit **16** for an ECL application requires configuration pin **22** (V_A) and configuration pin **24** (V_B) are connected to receive configuration signal, V_{CC}–2 volts. To terminate receiver circuit **16** for an CML application requires configuration pin **22** (V_A) and configuration pin **24** (V_B) are connected to to receive configuration signal, V_{CC}. LVDS termination for receiver circuit **16** requires configuration pin **22** (V_A) and configuration pin **24** (V_B) are connected together. Termination of the configuration pins **22, 24** is done external to receiver package **14**.

FIG. **2** illustrates an embodiment of a driver circuit and a receiver circuit system used in a single-ended configuration. The single-ended configuration receives a logic input signal at driver circuit **30**. Driver circuit **30** is a device from a typical logic family, e.g. ECL, CML, LVDS, CMOS, and TTL, or can be an analog driver circuit. Driver circuit **30** provides a signal boost for the logic input signal. Line **36** is connected to the output of driver circuit **30** to transmit a signal from driver circuit **30** to receiver package **32**. Receiver package **32** is a semiconductor package for receiver circuit **34**. V_{CC} and V_{EE} are power supply potentials to receiver package **32** providing power to receiver circuit **34**. Receiver circuit **30** is typically a differential receiver circuit amplifier manufactured as a semiconductor die. Receiver circuit **30** and receiver package **32** are an integrated receiver circuit.

Receiver circuit **34** receives two input signals: an information signal from driver circuit **30** on terminal **36**, and control signal IN on terminal **37**. Receiver circuit **34** is terminated at terminal **36** with load element **40**, and at terminal **37** with load element **38**. Load element **38** is connected to configuration pin **44** and load element **40** is connected to configuration pin **42**. Load elements **38, 40** are

resistors contained within receiver package **32** having a resistance of 50, 75, or 100 ohms. Configuration pins **42**, **44** are external pins connected to receiver package **32** and are programmable so receiver circuit **34** can communicate with different logic family drivers. Configuration pins **42**, **44** are programmed by terminating the pins using a configuration which is dependent on the desired logic family application. The configuration of receiver circuit **34** is controlled by connecting configuration pin **42** (V_C) and configuration pin **44** (V_D) as follows.

ECL:	$V_C = V_{CC} - 2$ volts V_D = open IN = V_{BB}
CMOS:	V_C = open V_D = open IN = $V_{CC}/2$
TTL:	V_C = open V_D = open IN = 1.5 volts

V_{BB} is typically the middle of an output swing to an ECL output. To terminate receiver circuit **34** for an ECL application requires configuration pin **42** (V_C) is connected to receive configuration signal, $V_{CC}-2$, configuration pin **44** (V_D) is devoid of a configuration signal, i.e. is left open, and terminal **37** is connected to receive control signal, V_{BB}. To terminate receiver circuit **34** for a CMOS application requires configuration pin **42** (V_C) and configuration pin **44** (V_D) are devoid of a configuration signal, and terminal **37** is connected to receive control signal, $V_{CC}/2$. TTL termination for receiver circuit **34** requires configuration pin **42** (V_C) and configuration pin **44** (V_D) are devoid of a configuration signal, and terminal **37** is connected to receive control signal, 1.5 volts. Termination of the configuration pins **42**, **44** is done external to receiver package **32**.

FIG. **3** illustrates an embodiment of a driver circuit and a receiver circuit system used in a modified single-ended configuration. The single-ended configuration receives a logic input signal at driver circuit **50**. Driver circuit **50** is a device from a typical type of logic family, e.g. ECL, CML, LVDS, CMOS, and TTL, or can be an analog driver circuit. Driver circuit **50** provides a signal boost for the logic input signal. Receiver package **52** receives a drive signal on line **56** from driver circuit **50**. Receiver package **52** is a semiconductor package for receiver circuit **54**. V_{CC} and V_{EE} are power supply potentials to receiver package **52** providing power to receiver circuit **54**. Receiver circuit **54** is terminated with load element **58** which is connected to configuration pin **60**. Load element **58** is a resistor contained within receiver package **52** having a resistance of 50, 75, or 100 ohms. Configuration pin **60** is an external pin connected to receiver package **52** that is programmable so receiver circuit **54** can communicate with different logic family drivers. Configuration pin **60** is programmed by terminating the pin using a configuration which is dependent on the desired logic family application. The configuration of receiver circuit **54** is controlled by connecting configuration pin **60** (V_E) as follows.

ECL:	$V_E = V_{CC} - 2$
CML:	$V_E = V_{CC}$
LVDS:	V_E = open

To terminate receiver circuit **54** for an ECL application requires that configuration pin **60** (V_E) is connected to receive configuration signal, $V_{CC}-2$. For a CML application, receiver circuit **54** is terminated with configuration pin **60** (V_E) connected to receive configuration signal, V_{CC}. LVDS termination for receiver circuit **54** requires that configuration pin **60** (V_E) be left open. Termination of the configuration pin **60** is done external to receiver package **52**.

FIG. **4** illustrates a differential configuration similar to FIG. **1**, except termination is done on driver package **70**. Driver circuit **72** is terminated at load element **74** and load element **76**. Load element **74**, **76** are resistors contained within driver package **70** having a value of 50, 75, or 100 ohms. Configuration pin **78** and configuration pin **80** are configured similar to table shown for the differential configuration in FIG. **1**. Driver circuit **72** provides an output signal on differential line **82** to receiver circuit **84**.

FIG. **5** illustrates a detailed schematic of the differential configuration in FIG. **1**. Semiconductor package **90** houses a leadframe **92** with metal leads similar to lead **94** which provide input and output signals. The input and output signals consist of differential input logic signals IN_1, and IN_2, differential output logic signals OUT_1, and OUT_2, power supply signals V_{CC} and V_{EE}, and configuration signals V_A and V_B on configuration pins **97**, **99** respectfully. Semiconductor die **96** is attached to flag **98** which is attached to leadframe **92**. Bond wire **100** is attached to bond pad **102** on semiconductor die **96** to provide electrical contact to bond pad **104** for the V_{EE} signal. All other input and output signals have the same bond wire configuration to provide electrical contact. The wire bonding technology used is typically a bump type technology or a ball grid array (BGA) technology. The differential configuration typically has differential amplifier **106** for receiver circuit **16** of FIG. **1**. Load elements **108**, **110** are connected to bond pads **112**, **114** respectfully to provide an electrical connection to configuration signals V_B and V_A. The differential signal from logic circuit **10** of FIG. **1** is received at lead **119** (IN_1) and lead **117** (IN_2) which has electrical contact to bond pads **118**, **116** on semiconductor die **96**, and to differential amplifier **106**. The logic output signal from receiver circuit **16** of FIG. **1** is coupled from differential amplifier **106**, electrical contact is made to bond pads **120**, **122** on semiconductor die **96**, and the signals are coupled to leads **121**. (OUT_1) and **94** (OUT_2) respectfully. Power supply is received at leads **125** (V_{CC}) and **126** (V_{EE}) making electrical contact to differential amplifier **106** through bond pads **124**, **102** respectively.

An alternative method to provide termination to any of the above embodiments is to use a switch between the termination (load) elements and the (configuration) termination signals. For example, FIG. **1** has external (configuration) termination pins **22**, **24** which are configured to receive different termination signals depending on the logic family application. A switch can be used to programmably connect termination pins **22**, **24** to $V_{CC}-2$ for an ECL logic family application, or to V_{CC} for a CML logic family application. The switch can provide programmability for the termination signals to any of the previous configurations outlined herein.

Thus, a technique for generating multiple input termination options on a single integrated circuit is disclosed. A receiver circuit is programmable to configure different termination connections which allow the receiver circuit to communicate with a driver circuit from a different logic family. The receiver circuit has at least one external configuration pin that is configured to provide the necessary termination for the type of logic family driver circuit used. The configuration pin is external to a semiconductor package housing the receiver circuit. Having configuration pins external to the semiconductor package provides for easy

portability among different logic families, and easy termination options which require no additional translators to operate a mixed logic family system.

What is claimed is:

1. An integrated logic circuit having a differential input receiving a differential signal, comprising:

a receiver having first and second inputs coupled for receiving the differential signal;

a semiconductor package for housing the receiver, having first and second pins respectively coupled to the first and second inputs of the receiver, and a supply pin coupled to the receiver for providing a power supply potential;

a first termination element housed in the semiconductor package and coupled between the first input of the receiver and a first programmable configuration pin of the semiconductor package; and

a second termination element housed in the semiconductor package and coupled between the second input of the receiver and a second programmable configuration pin of the semiconductor package, wherein the first and second programmable configuration pins receive first and second termination signals to configure termination for the logic circuit.

2. The integrated logic circuit of claim **1**, wherein the first and second termination elements comprise resistors.

3. A method of configuring a receiver circuit using first and second configuration signals, and receiving first and second input signals to the receiver circuit, comprising:

coupling an information signal on the first input to the receiver circuit;

coupling a control signal on the second input to the receiver circuit;

providing a first programmable configuration pin of a semiconductor package housing the receiver circuit;

connecting a first load element between the first input of the receiver circuit and the first programmable configuration pin;

providing a second programmable configuration pin of a semiconductor package housing the receiver circuit; and

connecting a second load element between the second input of the receiver circuit and the second programmable configuration pin.

4. The method of claim **3**, wherein the first and second programmable configuration pins receive a configuration selected from the group consisting of the first configuration signal, the second configuration signal, and devoid of the first and second configuration signals.

5. The method of claim **3**, wherein the second input receives a control signal selected from the group consisting of a first control signal, a second control signal, and a third control signal.

6. An integrated circuit, comprising:

a semiconductor package having first and second pins respectively adapted for receiving first and second data signals, third and fourth pins for respectively receiving first and second termination signals, and a supply pin coupled for receiving a power supply voltage; and

a semiconductor die housed in the semiconductor package for operating from the power supply voltage, and having a first load element coupled between the first and third pins to terminate the first data signal, and a second load element coupled between the second and fourth pins to terminate the second data signal.

7. The integrated circuit of claims **6**, wherein the first and second load elements are resistors.

8. The integrated circuit of claim **6**, wherein the semiconductor die includes a receiver circuit having first and second inputs coupled to the first and second pins, respectively.

9. The integrated circuit of claim **6**, wherein the semiconductor die includes a driver circuit having first and second outputs coupled to the first and second pins, respectively.

10. The integrated circuit of claim **6**, wherein the first data signal is from a first logic family, and the third pin is coupled for receiving a first termination voltage characteristic of the first logic family.

11. The integrated circuit of claim **10**, wherein the second data signal is from a second logic family, and the fourth pin receives a second termination voltage of the second logic family.

12. A method of operating an integrated circuit, comprising the steps of:

applying first and second logic signals to first and second pins, respectively, of a semiconductor package of the integrated circuit; and

loading the first and second logic signals with first and second load elements, respectively, of the integrated circuit, where the first and second load elements are coupled to third and fourth pins of the semiconductor package to provide a programmable termination for the first and second logic signals.

13. The method of claim **12**, wherein the first and second logic signals function as a differential signal and the third and fourth pins are for coupling together to terminate the differential signal.

14. The method of claim **12**, wherein the first and second logic signals are specified in accordance with first and second logic families and the third and fourth pins are coupled to first and second configuration signals of the first and second logic families, respectively.

15. The method of claims **14**, wherein the first and second logic signals are ECL signals referenced to a supply voltage, and the first and second configuration signals have values equal to the supply voltage minus about two volts.

16. The integrated logic circuit of claim **12**, further comprising the step of applying a power supply voltage to a fifth pin of the semiconductor package to bias the integrated circuit.

* * * * *

EXHIBIT C

US005361001A

United States Patent [19]

Stolfa

[11] Patent Number: 5,361,001

[45] Date of Patent: Nov. 1, 1994

[54] **CIRCUIT AND METHOD OF PREVIEWING ANALOG TRIMMING**

[75] Inventor: **David L. Stolfa**, Phoenix, Ariz.

[73] Assignee: **Motorola, Inc.**, Schaumburg, Ill.

[21] Appl. No.: **160,762**

[22] Filed: **Dec. 3, 1993**

[51] **Int. Cl.**[5] **H03K 3/01**; H03B 1/04

[52] **U.S. Cl.** **327/530**; 327/525; 327/312

[58] **Field of Search** 307/202.1, 296.1, 547, 307/548

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,158,786 6/1979 Hirasawa 307/296.1
4,446,534 5/1984 Smith 307/202.1

FOREIGN PATENT DOCUMENTS

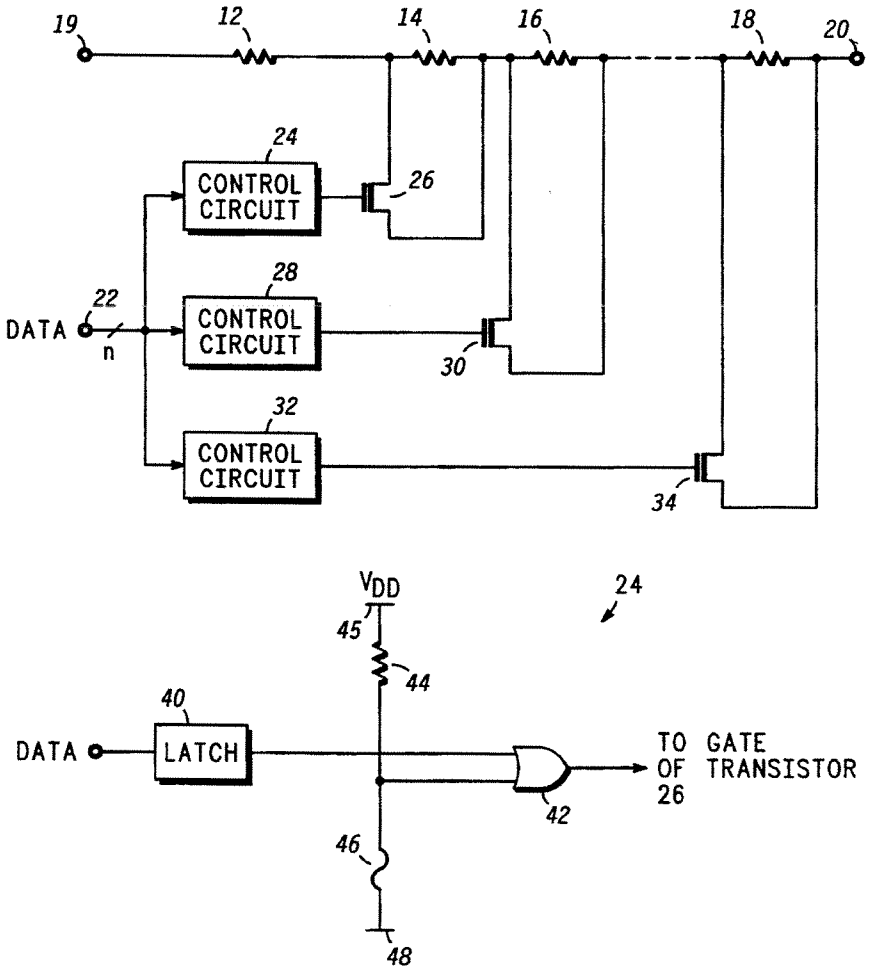
0112298 5/1987 Japan 307/202.1
0262716 10/1990 Japan 307/202.1

Primary Examiner—Margaret Rose Wambach
Attorney, Agent, or Firm—Robert D. Atkins

[57] **ABSTRACT**

An analog trim circuit enables and disables one or more serially connected passive elements for setting characteristics of the circuit. Each passive element has a transistor across its first and second conduction terminals operating in response to a control signal from a control circuit for enabling and disabling conduction through the associated passive element. The control circuits are responsive to a data signal for providing the control signals that enable and disable the conduction through the passive elements. The data signal allows a preview of the trimming results. The fuse in certain ones of the control circuits are blown to set the control signals to fixed values after removal of the data signal.

7 Claims, 1 Drawing Sheet



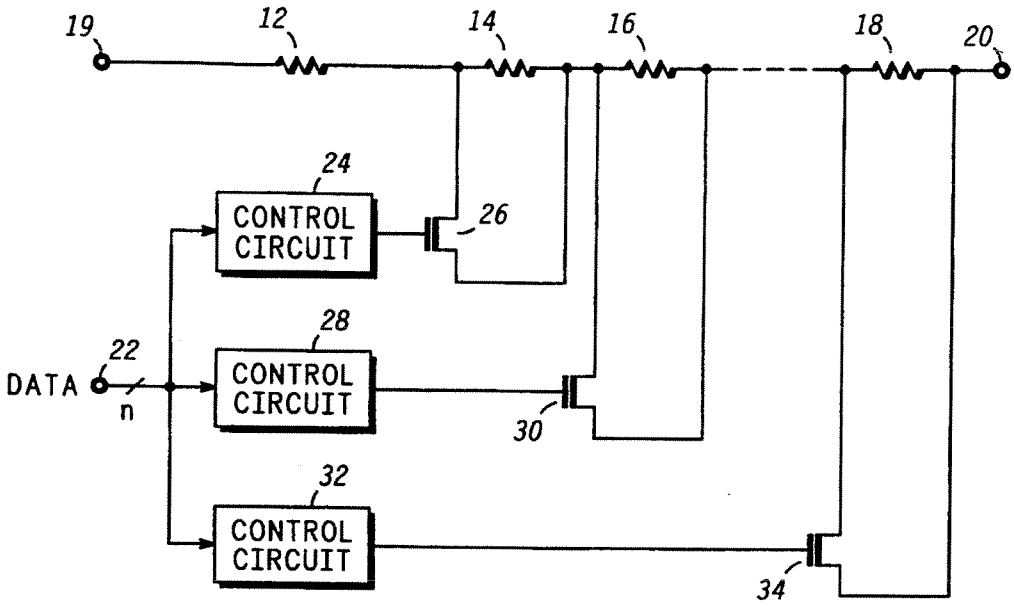
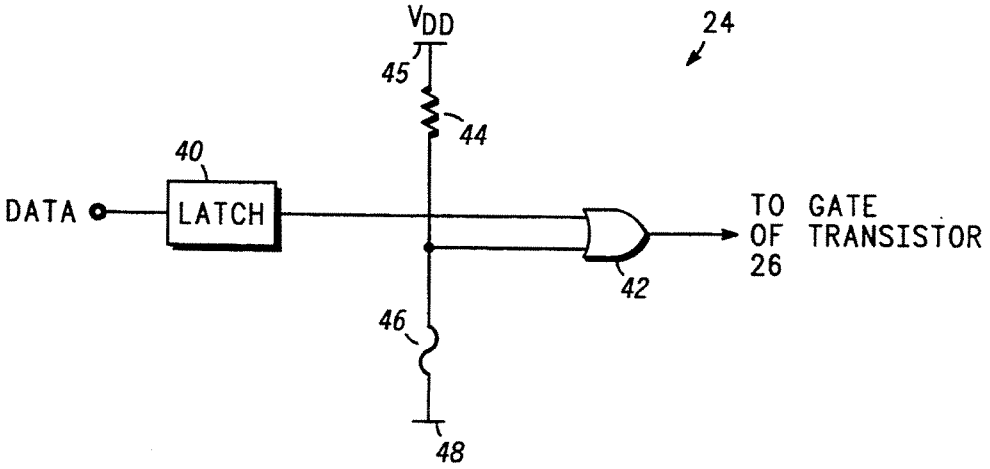

19
12
14
16
18
20
24
CONTROL CIRCUIT
26
28
CONTROL CIRCUIT
22
DATA
n
30
32
CONTROL CIRCUIT
34
10

FIG. 1

FIG. 2


V_{DD}
24
45
44
40
DATA
LATCH
TO GATE OF TRANSISTOR 26
42
46
48

CIRCUIT AND METHOD OF PREVIEWING ANALOG TRIMMING

BACKGROUND OF THE INVENTION

The present invention relates in general to analog trim circuits and, more particularly, to a technique of previewing the analog trim results before blowing a fuse to lock the trim in place.

In manufacturing analog integrated circuits, the basic building blocks are usually not accurately controlled by the manufacturing process as may be desired. For example, capacitors and resistors may have the wrong value, and MOS transistors may have the wrong gain setting. There are too many variables in the manufacturing process to yield absolute predictable results. Yet historically analog circuits often require very accurate voltage references, frequency references, and accurately ratioed elements.

To compensate for the process variability, many electronic circuits use analog trimming during test to set resistor values as necessary for proper operation of the circuit. A typical trimming technique utilizes a resistor ladder comprising a series of serially coupled resistors each in parallel with either a fuse or anti-fuse. A fuse is a device that is substantially an electrical short until it is blown open. An anti-fuse is an electrical open until blown when it becomes substantially an electrical short.

The fuse-blowing approach may take several forms, each with its own shortcomings. Laser fuses may be used directly across each resistor element in the ladder to enable and disable conduction through the resistor. During test, certain resistors are selected to open the shunt element thereby adding resistance to the serial path. The resistor ladder should be adjustable at wafer test over a range from say 10 to 2,560 ohms in 10 ohm increments.

The analog trimming may be performed iteratively, i.e. test, trim, test, trim, to measure the effect of the course trim and determine the necessary fine trimming. For iterative trimming, a laser trim system is typically installed on the wafer tester to alternately test and trim. However, one laser system per tester is very expensive. The laser is often in an idle state waiting for the tester. Moreover, if either the test system or laser breaks down both are inoperative.

An alternate approach is to use a zener anti-fuse across the resistor ladder. Such an element can be cheaply trimmed on the tester so that iterative testing can be done in one pass on the tester. Zener anti-fuses require large currents to program. Therefore, each anti-fuse requires its own external pad and probe card needle. This restricts the programming bit count to say 5–10 bits before the die area for test pads and complexity of the probe card requirements become prohibitive.

In general, iterative testing is a slow and expensive process. Consequently, many trimming techniques utilize only a single pass to evaluate which resistors in the serial string should be included to achieve the desired analog circuit operation. Thus, as result of a test measurement, the user blows the shunt fuse elements whereby the circuit is expected to operate as planned. The process of blowing the fuses typically involves laser trimming off-line from the test set to cut the poly material and open the shunt element. The circuit may be returned to the test set to verify proper trimming. If the subsequent testing should fail, the part is typically discarded since it is difficult to patch the shunt fuse elements.

Hence, a need exists for an iterative trimming to evaluate the results of test before permanently setting the trim.

BRIEF DESCRIPTION OF THE DRAWING

FIG. **1** is a block diagram illustrating an analog trimming circuit; and

FIG. **2** is a schematic diagram illustrating the control circuit of FIG. **1**.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

An analog trim circuit is shown in FIG. **1** including a passive ladder network **10** comprising resistors **12**, **14**, **16** and **18** serially coupled between terminal **19** and terminal **20**. Resistor **12** is non-trimmable and provides the minimum ladder resistance (R_{MIN}). Resistors **14–18** are selected in an exponential series, such as 1280, 640, 320, 160, 80, 40, 20, and 10 ohms. Resistors **14–18** are passive elements each with first and second conduction terminals. Other passive elements may also be used in the trim circuit. A data signal is applied at terminal **22**. One bit of the data signal is applied to each of control circuits **20**, **28** and **32**. An address signal selects the control circuit to latch one bit of the data signal.

Control circuit **24** provides a control signal to the gate of MOS transistor **26**. The drain and source of transistor **26** are coupled to first and second conduction terminals of resistor **14**. Likewise, control circuit **28** provides a control signal to the gate of MOS transistor **30** which has its drain and source coupled across resistor **16**. Control circuit **32** provides a control signal to the gate of MOS transistor **34**. The drain and source of transistor **34** are coupled across the first and second conduction terminals of resistor **18**. The effective resistance through resistor ladder **10** is thus temporarily set by transistors **26**, **30** and **34** selectively enabling and disabling conduction through resistors **14–18** upon receiving a high state or low state of control signals from control circuits **24**, **28** and **32**. With the above trimming scheme, the resistor ladder is controllable from R_{MIN} to $R_{MIN}+2{,}560$ ohms assuming eight trimmable resistors in 256 possible 10 ohm increments.

Turning to FIG. **2**, further detail of control circuit **24** is shown. Control circuits **28** and **32** follow a similar construction and operation as described for control circuit **24**. The data signal is latched in latching circuit **40** for application to a first input of OR gate **42**. An address signal enables latching circuit **40** to latch the data bit. Resistor **44** is coupled between the second input of OR gate **42** and power supply conductor **45**. Power supply conductor **45** operates at a positive potential VDD such as 5 volts. Fuse **46** is coupled between the second input of OR gate **42** and power supply conductor **48** operating at ground potential. The output of OR gate **42** provides the control signal to the gate of transistor **26**. An alternate embodiment of control circuit **24** may replace OR gate **42** with a NAND gate while resistor **44** and fuse **46** exchange places in the circuit.

Trim circuits are used in a variety of applications. For example, a circuit may require a given frequency f_o determined by an RC time constant such that the frequency is inversely proportional to RC. The resistance R and capacitance C should be selected such that the nominal process target values of sheet ρ (resistance per

unit area) and capacitance per unit area yield the desired frequency f_o. However, the actual process values of resistance and capacitance may vary by 5%–10%. Thus, the trimmable resistor ladder **10** must be trimmed to compensate for any variation in sheet ρ and capacitance per unit area.

During testing at wafer level, the circuit under test is exercised and any correction necessary to resistor ladder **10** is calculated by a binary search. Steps are taken to determine whether a resistor should be trimmed such that it is in the upper half or lower half of its trimmable range, i.e. determining if the most significant bit or largest resistor should be shorted or left to remain in resistor ladder **10**. With resistor ladder **10** trimmed to its most significant bit the circuit under test is again tested and a correction is calculated to determine if it should be trimmed to the upper half or lower half of the remaining trimmable range. As a result, the next most significant resistor is shorted or allowed to remain. The process continues until all trimmable resistors have been checked.

Consider the trimming operation during test where a logic one data signal is stored in latching circuit **40** of each of control circuits **24**, **28** and **32**. The output of each OR gate **42** goes high and enables transistors **26**, **30** and **34**. Resistors **14–18** are substantially shorted, i.e. disabling the conduction path through resistors **14–18**. The resistance of ladder **10** is equal to R_{MIN}.

To perform trim preview during test, the data signal to control circuit **24** is set to logic zero and stored in its latching circuit **40**. At wafer test all fuses are yet unblown so that all fuse inputs to the OR-gates are low. The control signal at the output of OR-gate **42** goes low and turns off transistor **26** to enable the conduction through resistor **14**. The resistance of ladder **10** increases to $R_{MIN}+R_{14}$, where R_{14} is the value of resistor **14**. The effect of the added resistance on the operation of the circuit under test may be checked and verified by the tester. If more resistance is needed, the data signal to control circuit **28** may be set to logic zero. The control signal to transistor **30** goes low as described above for control circuit **24**. Transistor **30** turns off and enables the conduction through resistor **16**. The resistance of ladder **10** increases to $R_{MIN}+R_{14}+R_{16}$, where R_{16} is the value of resistor **16**. Again, the effect of the added resistance on the operation of the circuit under test may be checked and verified by the tester. The process continues until the circuit under test operates as desired. Note at this point, the trimming process is temporary and dependent on the data signals to control circuits **24**, **28** and **32**. No fuses have yet been blown to lock in the trim. Thus, different combinations of resistors **14–18** may be previewed and checked to achieve optimal results.

An alternate trim approach could initially set the data signals to logic zero in control circuits **24**, **28** and **32**. The output of each OR gate **42** goes low and disables transistors **26**, **30** and **34**. The shunt elements **26**, **30** and **34** are substantially opened, i.e. enabling conduction through resistors **14–18**, thereby making ladder **10** resistance maximum. The testing preview involves setting the data signals to logic one and iteratively enabling transistors **26**, **30** and **34** to disable conduction through resistors **14–18** and reduce resistance in ladder **10**. The process continues until the circuit under test operates as desired. Again, the trimming process is temporary and dependent on the data signals to control circuits **24**, **28** and **32**. No fuses have yet been blown to lock in the trim. Different combinations of resistors **14–18** may be tried and checked to achieve optimal results.

Another embodiment of the present invention is to configure the resistor ladder with the resistors in parallel and the control transistors in series with each resistor.

For the circuits under test that functionally pass, the bit pattern of trim is recorded in a file by wafer and die site. The file accompanies the wafer to a laser fuse system where the selected fuses **46** are blown. Once the appropriate fuses are blown, the latches in the control circuits are set to logic zero so that the state of the fuses alone determines the state of the control signal and therefore the permanent trim. The control signals from control circuits **24**, **28** and **32** are thus set to a fixed value by blowing the selected fuses **46** in the control circuits after removal of the data signal at terminal **22**.

The fuses are generally doped polycrystalline silicon films sometimes silicided polycrystalline silicon films in the range of 10 to 500 ohms. The polysilicon film is usually made in the shape of a polysilicon resistor with a width five to ten times its length. The ends of the fuses are connected by metal interconnects to the relevant circuitry. The fuse usually has most or all overlying oxide layers removed. With the use of on-die alignment marks the laser beam of approximately 1 μm–2 μm beam width is focused on the center of the fuse. The laser beam is a pulsed signal of such an energy that the polysilicon is vaporized and the fuse is severed and therefore permanently no longer conductive.

A key feature of the present invention is to preview trimming at wafer test to provide an economical means of iteratively trimming the resistive ladder using data provided by the tester. A data signal selectively trims the resistor ladder. The trimming is temporary and may be modified with different data signals to achieve optimal results. When the proper pattern of trim bits is determined for each individual circuit under test, that data is recorded and transferred off-line to the laser trimmer along with the wafer. The laser trim system blows the appropriate fuses for each circuit under test according to the pattern previously determined by testing various trimming options. Once the appropriate fuses are blown, the latches in the control circuits are set to logic zero so that the state of the fuses alone determines the state of the control signal and therefore sets the permanent trim. The preview trimming process allows optimization of the bit pattern for trimming before the actual laser trimming. Furthermore, the testing and the fusing systems may remain separate without requiring multiple passes through each.

While specific embodiments of the present invention have been shown and described, further modifications and improvements will occur to those skilled in the art. It is understood that the invention is not limited to the particular forms shown and it is intended for the appended claims to cover all modifications which do not depart from the spirit and scope of this invention.

I claim:

1. An analog trim circuit, comprising:

a passive element having first and second conduction terminals;

first means coupled across said passive element and operating in response to a control signal for enabling and disabling conduction through said passive element, said first means includes a transistor having a gate, a drain and a source, said drain being coupled to said first conduction terminal, said

source being coupled to said second conduction terminal, said gate being coupled for receiving said control signal; and

second means responsive to a data signal for providing said control signal to said first means to enable and disable said conduction through said passive element, said second means setting said control signal to a fixed value after removal of said data signal.

2. The analog trim circuit of claim 1 wherein said passive element includes a first resistor coupled between said first and second conduction terminals.

3. The analog trim circuit of claim 2 wherein said second means includes:

a latching circuit having an input coupled for receiving said data signal and having an output;

a logic gate having first and second inputs and an output, said first input being coupled to said output of said latching circuit, said output being coupled for providing said control signal;

a second resistor coupled between a first power supply conductor and said second input of said logic gate; and

a fuse coupled between said second input of said logic gate and a second power supply conductor.

4. A method of analog trimming, comprising the steps of:

enabling conduction through a passive element in response to a first state of a control signal;

disabling conduction through said passive element in response to a second state of said control signal;

activating said control signal in response to a data signal to enable and disable said conduction through said passive element, said activating step including the steps

(a) latching said data signal, and

(b) logically combining said data signal with a logic signal for providing said control signal; and

setting said control signal to a fixed value after removal of said data signal.

5. The method of claim 4 wherein said setting step includes the steps of:

removing said data signal; and

blowing a fuse to set said control signal at said fixed value.

6. An analog trim circuit, comprising:

a passive element having first and second conduction terminals;

a transistor having a gate, a drain and a source, said drain being coupled to said first conduction terminal, said source being coupled to said second conduction terminal, said gate being coupled for receiving a control signal;

a latching circuit having an input coupled for receiving a data signal and having an output;

a logic gate having first and second inputs and an output, said first input being coupled to said output of said latching circuit, said output being coupled for providing said control signal;

a first resistor coupled between a first power supply conductor and said second input of said logic gate; and

a fuse coupled between said second input of said logic gate and a second power supply conductor.

7. The analog trim circuit of claim 6 wherein said passive element includes a first resistor coupled between said first and second conduction terminals.

* * * * *

EXHIBIT D

United States Patent [19]

Schuster et al.

[11] **Patent Number: 5,000,827**

[45] **Date of Patent: Mar. 19, 1991**

[54] **METHOD AND APPARATUS FOR ADJUSTING PLATING SOLUTION FLOW CHARACTERISTICS AT SUBSTRATE CATHODE PERIPHERY TO MINIMIZE EDGE EFFECT**

[75] Inventors: **Virgil E. Schuster; Reginald K. Asher, Sr.,** both of Scottsdale; **Bhagubhai D. Patel,** Tempe, all of Ariz.

[73] Assignee: **Motorola, Inc.,** Schaumburg, Ill.

[21] Appl. No.: **459,892**

[22] Filed: **Jan. 2, 1990**

[51] **Int. Cl.**[5] **C25D 5/02**

[52] **U.S. Cl.** **204/15**

[58] **Field of Search** 204/15

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,287,029 9/1981 Shimamura 204/15

FOREIGN PATENT DOCUMENTS

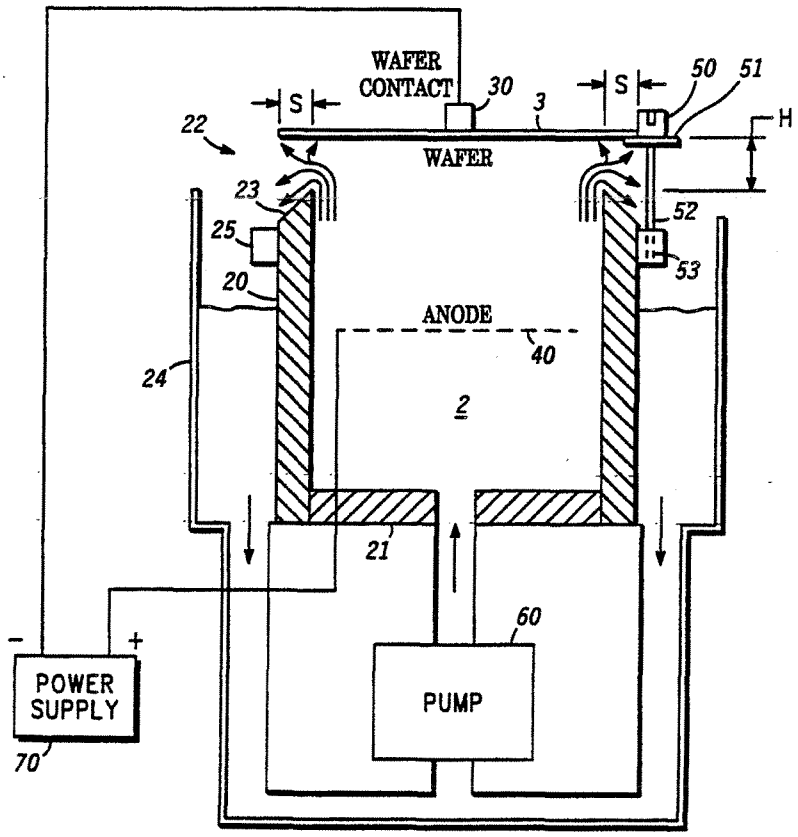
28039 3/1978 Japan .
123089 5/1989 Japan .
198017 8/1989 Japan .
242797 9/1989 Japan .

Primary Examiner—T. M. Tufariello
Attorney, Agent, or Firm—Charles R. Lewis; Walter W. Nielsen

[57] **ABSTRACT**

A method and apparatus for electroplating metallized bumps of substantially uniform height on predetermined terminal areas of a substrate. Cup plating apparatus includes elements for adjusting parameters affecting the geometry of the substrate relative to the plating cup, as well as flow rate of the electroplating solution against the substrate surface. By achieving non-laminar flow of the electroplating solution near the substrate edges, the plating characteristics of the electroplating solution are altered in this region, substantialy offsetting "edge effect", so that the resulting plated bump height is substantially uniform across the substrate.

2 Claims, 7 Drawing Sheets



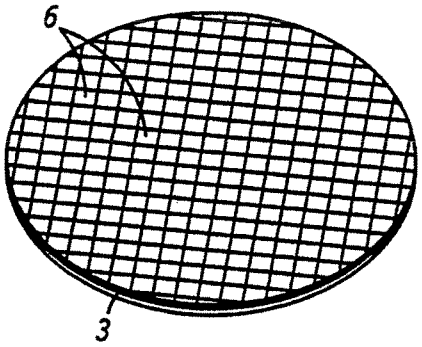


FIG. 1

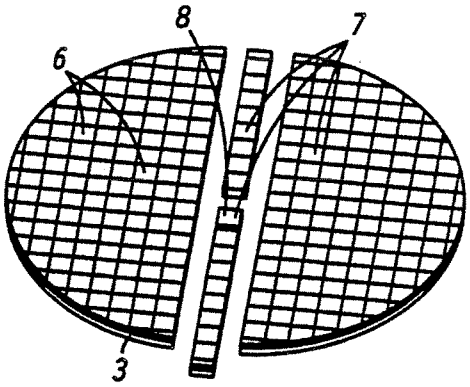


FIG. 2

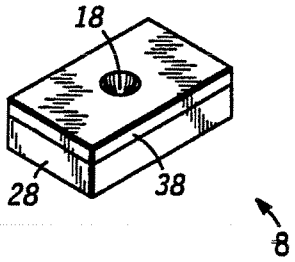


FIG. 3A

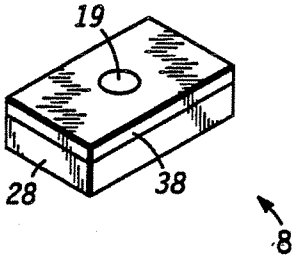


FIG. 3B

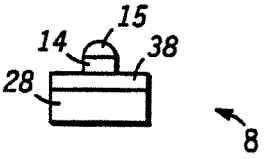


FIG. 3C

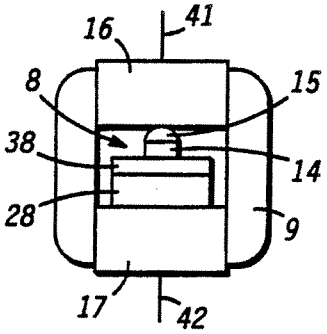


FIG. 4

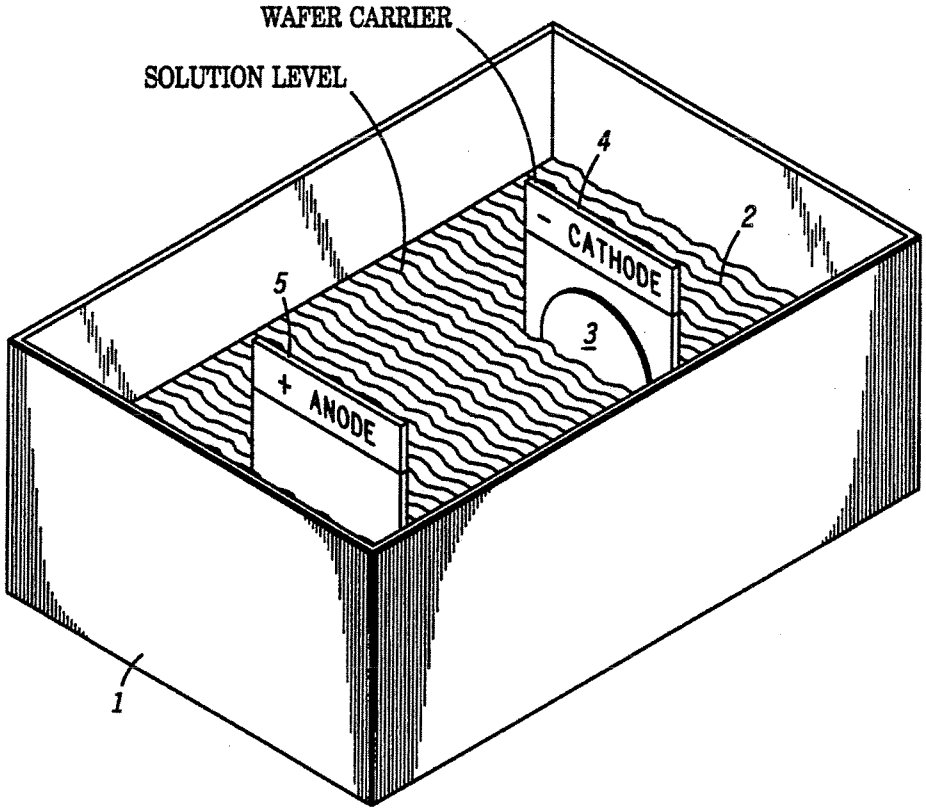
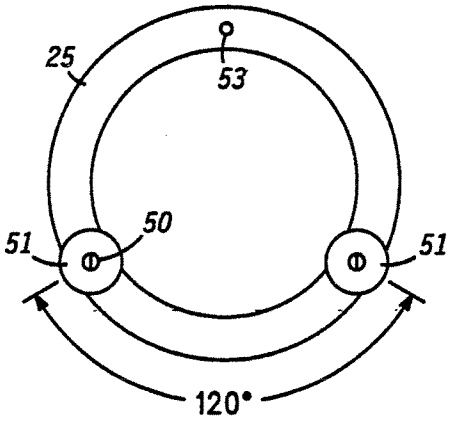


FIG. 5
-PRIOR ART-

FIG. 8



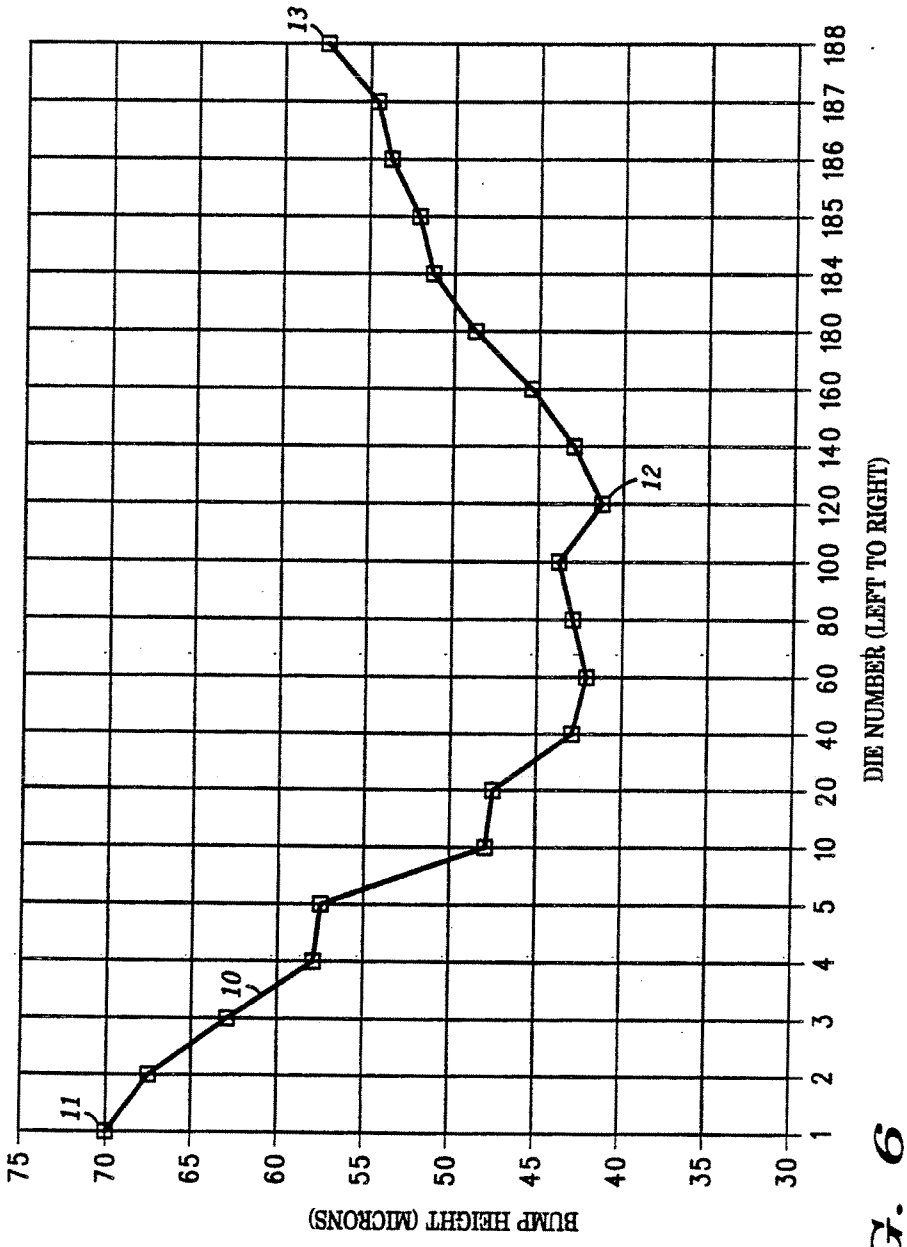

13
12
11
10
75
70
65
60
55
50
45
40
35
30
1
2
3
4
5
10
20
40
60
80
100
120
140
160
180
184
185
186
187
188
BUMP HEIGHT (MICRONS)
DIE NUMBER (LEFT TO RIGHT)

FIG. 6

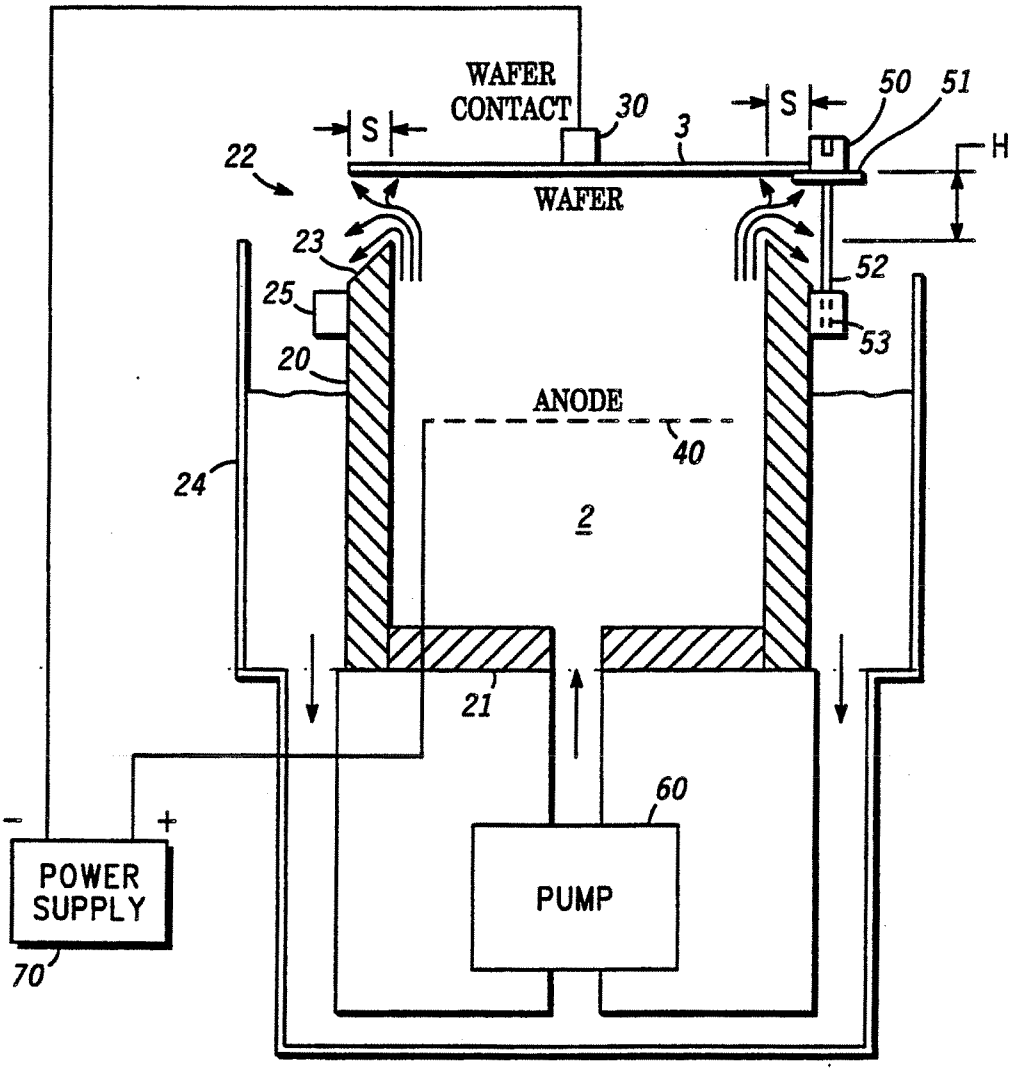

WAFER
CONTACT
30
3
S
S
50
51
H
22
WAFER
23
25
52
53
20
ANODE
40
24
2
21
60
POWER
SUPPLY
PUMP
70

FIG. 7

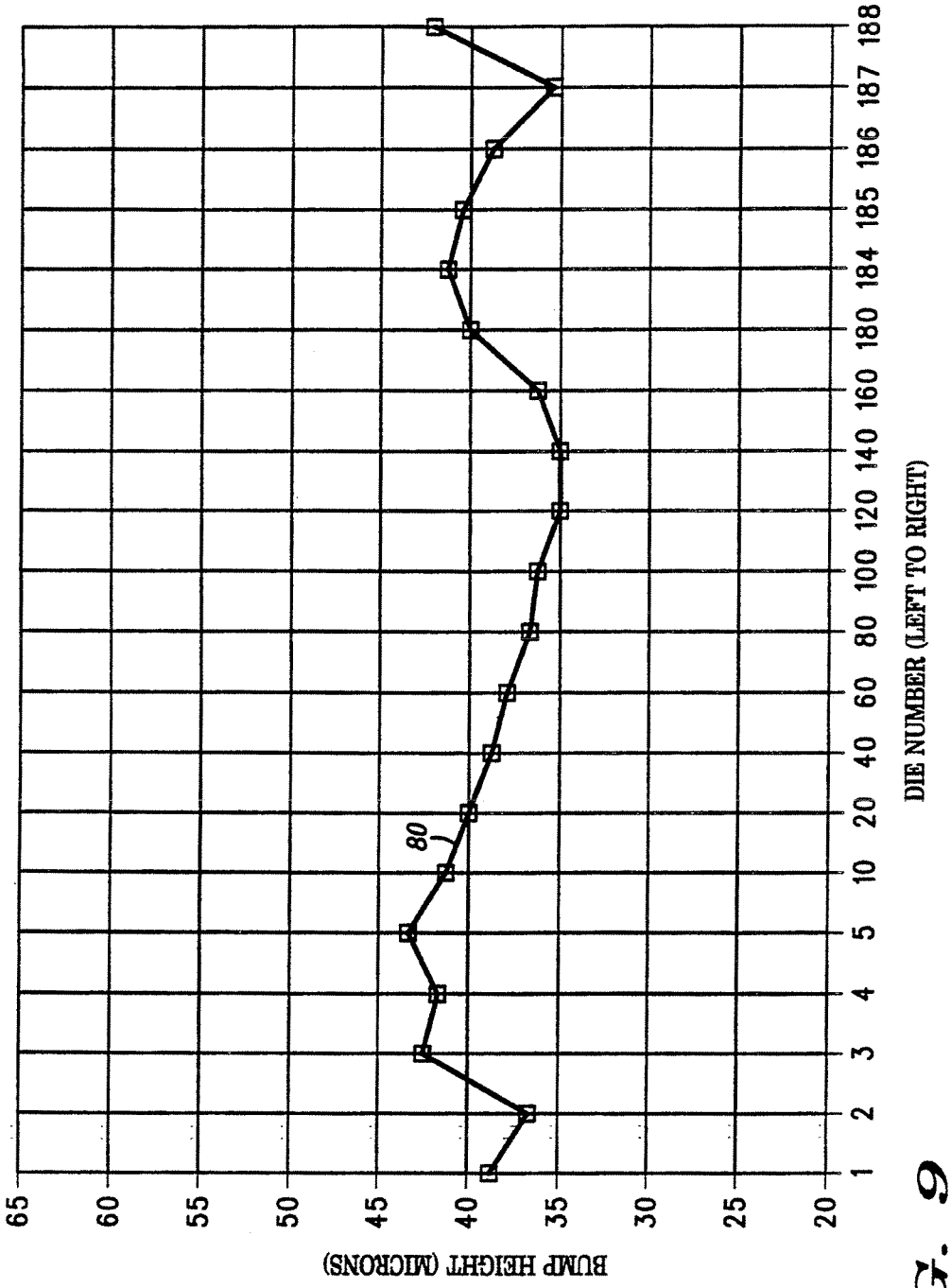

BUMP HEIGHT (MICRONS)
65
60
55
50
45
40
35
30
25
20
1
2
3
4
5
10
20
40
60
80
100
120
140
160
180
184
185
186
187
188
DIE NUMBER (LEFT TO RIGHT)
80

FIG. 9

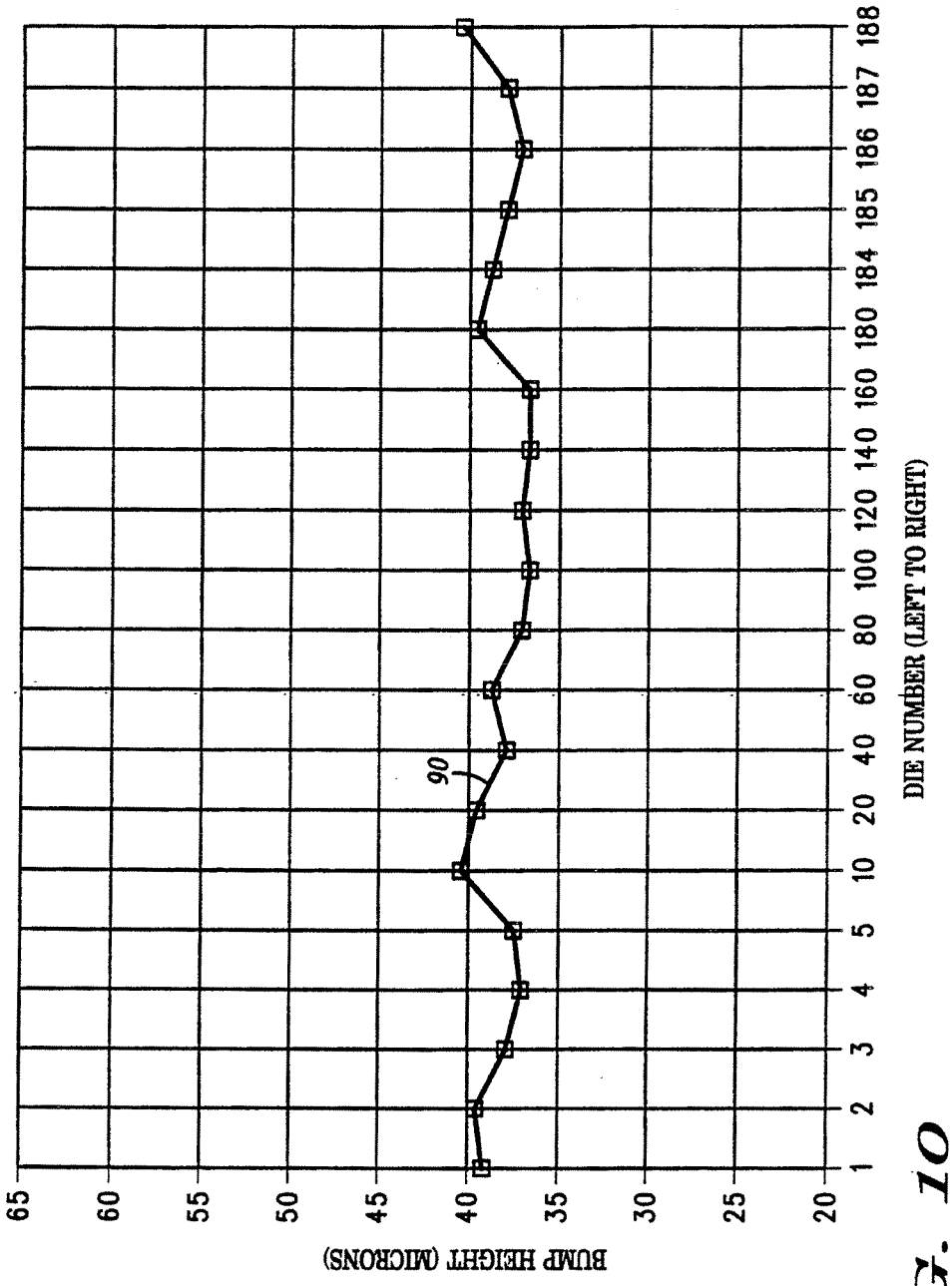

BUMP HEIGHT (MICRONS)
65
60
55
50
45
40
35
30
25
20
90
DIE NUMBER (LEFT TO RIGHT)
1
2
3
4
5
10
20
40
60
80
100
120
140
160
180
184
185
186
187
188

FIG. 10

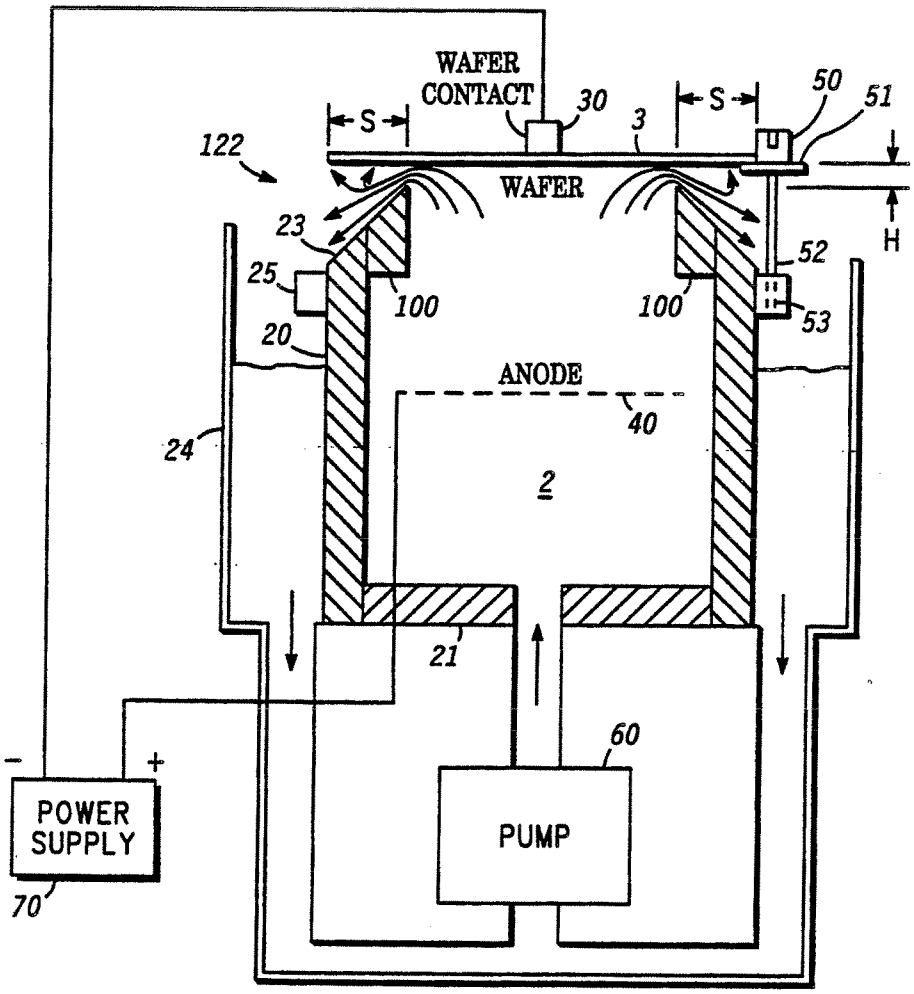

WAFER CONTACT
30
3
S
S
50
51
122
WAFER
H
23
25
100
100
52
53
20
ANODE
40
24
2
21
60
POWER SUPPLY
PUMP
70

FIG. 11

METHOD AND APPARATUS FOR ADJUSTING PLATING SOLUTION FLOW CHARACTERISTICS AT SUBSTRATE CATHODE PERIPHERY TO MINIMIZE EDGE EFFECT

BACKGROUND OF THE INVENTION

1. Technical Field of the Invention

This invention relates generally to the manufacture of micro-electrical circuits, and, more particularly, to the formation of uniform-thickness metallization bumps on terminal areas of electrical circuits on a substantially planar substrate, particularly near the edge thereof.

2. Background Information

The present invention has utility in the plating of metallization bumps on predetermined terminal areas of silicon wafers prior to scribing such wafers into a plurality of individual die.

FIG. 1 shows a silicon wafer 3 upon which a plurality of individual electrical circuit elements 6 are formed. The electrical characteristics of individual circuit elements 6 may be imparted to them by employing any suitable process(es) therefor. The specifics of the electrical circuit of the circuit elements 6 lies outside of the scope of the present invention.

FIG. 2 shows a view similar to that shown in FIG. 1, wherein the wafer 3 has been separated into pieces 7 including at least one die 8 using conventional wafer scribing or sawing techniques.

FIGS. 3A show steps in the formation of a terminal region 19 on a surface of an individual die 8, prior to wafer scribing or sawing, and the plating of a metallization bump onto such terminal region 19. In the manufacture of a particular electrical product from die 8, such as the double-slug diode shown in FIG. 4, it is frequently necessary to deposit a metallized bump in a predetermined area of a surface of such die.

Referring to FIG. 3A, a representative individual die 8 of wafer 3 is shown overlaid with a layer of oxide 38, and a hole or window 18 has been etched through the oxide 38 down to a terminal area (not shown) of the underlying substrate 28.

In FIG. 3B, the window 18 of FIG. 3A has been filled with top metal 19. In a preferred embodiment of the invention, the top metal 19 actually comprises three layers: first a layer of titanium, next a layer of nickel, and finally a layer of silver. Again, the composition of the layers and thickness thereof are not specific to the present invention.

In FIG. 3C, a metallization bump, comprising a layer of silver 14 and a layer of tin 15, has been electro-deposited over the top metal terminal region 19.

FIG. 4 shows a double-slug diode manufactured according to the method and apparatus disclosed by the present invention. The diode of FIG. 4 is shown for illustrative purposes only, and it should be understood by all practitioners in the art that the present invention has broad utility in many metallization bump processing applications and is not intended to be limited to implementations such as that shown in FIGS. 3 and 4.

Still with reference to FIG. 4, the die 8 has been separated from its counterparts on wafer 3 and mounted between copper "slugs" or terminals 16 and 17 to which electrical leads 41 and 42, respectively, have been affixed. The entire assembly is enclosed in glass 9.

FIG. 5 shows a prior art plating apparatus for plating metallization bumps onto predetermined terminal areas of a silicon wafer, such as terminal area 19 of die 8. Referred to as a rack plating apparatus, it comprises a tank 1 of electroplating solution into which an anode 5 and a cathode 4 are shown partially submersed. It will be understood that anode 5 and cathode 4 are shown partially submersed for ease in understanding and that during operation they are substantially submersed.

Anode 5 has a potential having a positive polarity coupled thereto, while cathode 4 has a potential having a negative polarity coupled thereto.

Affixed to cathode 4 is a substantially planar, conductive wafer 3 comprising a plurality of individual electrical elements (not shown), each with a terminal area such as terminal area 19 shown in FIG. 3B. It will be understood by those skilled in the art that substrate 3 may itself serve as the cathode 4, or substrate 3 may be suitably affixed to a wafer carrier, which serves as the cathode 4.

FIG. 6 is a graph illustrating the variation of bump height across a silicon wafer electroplated with the prior art plating apparatus shown in FIG. 5. The bump height in microns measured on selected die is provided along the Y-axis, and the die position across a given wafer diameter is provided along the X-axis. It will be observed that the X-axis of FIG. 6 is non-linerar, in that emphasis is given to die numbers closest to the wafer edge, for example die numbers 1–5 at the left edge and die number 184–188 at the right edge.

It is seen that when metallized bumps are plated with the apparatus shown in FIG. 6 there is substantial variation in bump height across the wafer diameter. The bumps are highest at or near the wafer edge. For example, the bump height 11 of die #1 is 70 microns, and that of die #188 is approximately 58 microns, whereas that of die #120 is approximately 41 microns.

According to the graph of FIG. 6, the bump height variation across a typical 9.65 centimeter diameter wafer is almost 30 microns, ranging from a minimum of 41 microns at die #120 to a maximum of 70 microns at die #1. This greatly exceeds a desired production specification width of 20 microns.

The increased electroplating intensity near the wafer edge is commonly referred to as "edge effect".

Therefore, there is a substantial need to provide an electroplating method and apparatus which overcomes the "edge effect" problem known in prior electroplating systems.

Various electroplating systems are known which have attempted to overcome the "edge effect". One such system is referred to as a cathode-mask system, in which the high-growth area of the substrate is masked. However, this system suffers from the need to achieve critcal positioning of the mask relative to the high-growth area of the substrate. Both the alignment of the mask and the mask-to-wafer spacing are critical and difficult to control.

BRIEF SUMMARY OF INVENTION

The present invention solves the problem of "edge effect" by selectively altering the metallic ion concentration of the electroplating solution near the edge(s) of the wafer substrate.

According to the present invention, the electroplating solution is contained in a cup-shaped container. A pump circulates the solution through an inlet and out over the lip of the cup. The wafer is suspended at an optimum height above the cup lip. The cup diameter is optimized relative to the wafer diameter and to the area

in which undue bump growth occurs. In addition, the flow rate of solution through the plating cup is optimized. By optimizing the above-mentioned parameters, the metallic ion concentration of the electroplating solution in the vicinity of the wafer edge(s) is optimized to just offset the "edge effect", and to provide substantially uniform height of electroplated bumps across the wafer diameter.

Accordingly, it is an object of the present invention to provide an electroplating method and apparatus which produce metallized bumps of substantially uniform height across a substrate including the edge(s) thereof.

Thus a greater proportion of die fall within desired specifications, resulting in lower rejection rates, lower material and labor charges, higher quality, and greater customer acceptance.

It is another object of the present invention to provide an electroplating method and apparatus which is relatively inexpensive and which is relatively easy to control.

It is yet another object of the present invention to provide an electroplating method and apparatus which eliminates the labor-intensive steps of mounting a substrate on a wafer carrier prior to electrodepositing the metallized bumps, demounting the substrate from the wafer carrier after deposition, and cleaning the mounting agent (typically wax, glycol, or plastic) from the substrate.

These and other objects are achieved in accordance with a preferred embodiment of the invention by providing a method of forming metallization bumps on predetermined terminal areas of a planar substrate, the bumps being of substantially uniform height across the substrate, wherein the method comprises (a) providing a planar substrate having thereon a multiplicity of terminal areas; (b) applying an electrical potential having a first electrical polarity to the terminal areas; (c) applying an electrical potential having a second electrical polarity to an electrical terminal immersed in a container of an electroplating solution; (d) exposing the substrate to the electroplating solution to permit the growth of the metallization bumps on the terminal areas: and (e) controlling the growth of the metallization bumps in a predetermined region of the substrate by altering the metallic ion concentration of the electroplating solution in the predetermined region.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention is pointed out with particularity in the appended claims. However, other features of the invention will become more apparent and the invention will be best understood by referring to the following detailed description in conjunction with the accompanying drawings in which:

FIG. 1 shows a silicon wafer upon which a plurality of individual electrical circuit elements are formed.

FIG. 2 shows a view similar to that shown in FIG. 1, wherein the wafer has been separated into pieces including at least one die.

FIGS. 3A, 3B and 3C show steps in the plating of a metallization bump onto a terminal area of an individual die.

FIG. 4 shows a double-slug diode manufactured according to the method and apparatus disclosed by the present invention.

FIG. 5 shows a prior art plating apparatus for plating metallization bumps onto predetermined terminal areas of a silicon wafer.

FIG. 6 is a graph illustrating the variation of bump height across a silicon wafer electroplated with the prior art plating apparatus shown in FIG. 5.

FIG. 7 shows a cross-sectional view of apparatus for plating metallization bumps of substantially uniform height onto predetermined terminal areas of a silicon wafer, according to the present invention.

FIG. 8 shows a top-view of ring element 25 and adjustable wafer support elements 51 of the plating apparatus shown in FIG. 7.

FIG. 9 is a graph illustrating the variation of bump height across a silicon wafer electroplated according to the method of the present invention.

FIG. 10 is another graph illustrating the variation of bump height across a silicon wafer electroplated according to the method of the present invention.

FIG. 11 shows a cross-sectional view of an alternative embodiment of apparatus for plating metallizaton bumps of substantially uniform height onto predetermined terminal areas of a silicon wafer, according to the present invention.

DESCRIPTION OF PREFERRRED EMBODIMENT

FIG. 7 shows apparatus for plating metallization bumps of substantially uniform height onto predetermined terminal areas of a silicon wafer, according to the present invention. A cylcindrical cup 20 of suitable material, such as polyvinylchloride (PVC) or polypropylene, contains the desired electroplating solution, which in a preferred embodiment is a cyanide silver plating solution. The bottom portion of cup 20 may be formed integrally therewith or may be formed separately, as shown by bottom portion 21.

Pump 60 circulates the plating solution 2 through an inlet in the bottom cup 20, and plating solution 2 exists cup 20 over the lip 23 into tank or sump 24, from which it is eventually returned to the inlet side of pump 60.

To a suitable power supply 70, such as a pulsing DC rectifier, are coupled a wafer contact 30 and an anode 40. Anode 40 may take the form of a platinum-clad tantalum screen immersed in the electroplating solution. Wafer contact 30 may take the form of a silver-clad nickel element which rests upon or is affixed to the upper surface of water or substrate 3. Wafer 3 functions as a cathode.

Wafer 3 is supported by several wafer support members 51 suitably mounted in a ring or collar member 25 around the periphery of cup 20 (refer to FIG. 8). Support member 25 may take the form of a PVC washer mounted on a PVC screw 52, having a slotted head 50, and being threaded into a mating opening 53 in ring 25.

FIG. 8 shows a top-view of ring element 25 and adjustable wafer support elements 51 of the plating apparatus shown in FIG. 7. In a preferred embodiment, three wafer support elements 51 are spaced substantially equidistantly around the periphery of ring 25, and each has a slotted head to facilitate adjusting the height of wafer 3 above the lip 23 of cup 20.

Operation of Preferred Embodiment

In operation, as mentioned above, electroplating solution 2 flows generally upwards from the inlet in the bottom of cup 20, against the underside of wafer 3, and out over the lip 23 into sump 24.

Cup plating apparatus is known in the art and, as used, suffers from the well-known "edge effect". However, according to the present invention the metallic ion concentration of electroplating solution **2** is altered in the region near the edge of wafer **3**, so as to effectively offset the "edge effect".

By creating non-laminar flow of the electroplating solution **2** through the opening between the lip **23** and lower surface of wafer **3**, the plating characteristics of solution **2** near the edge are altered from those elsewhere within cup **20**. The plating effect of the solution is weakened, thereby offsetting the tendency for increased plating effect near the cathode edge. The precise reasons as to why turbulent flow of the electroplating solution **2** against the outer portions of wafer **3** causes an offsetting of the "edge effect" are not completely understood.

To produce the non-laminar flow over the optimum peripheral area of wafer **3**, the distance S between the outer edge of wafer **3** and the inner surface of cup **20** should be optimized. The parameter S is changed by changing the diameter of cup **20** relative to the diameter of wafer **3**. By decreasing the diameter, a relatively greater peripheral area of wafer **3** is affected by a slight reduction in bump growth rate, whereas increasing the diameter of cup **20** diminishes the peripheral area of wafer **3** which is affected. In a preferred embodiment of the invention, the diameter of the wafer was 9.65 centimeters, and the inside diameter of the cup was 8.89 centimeters.

Another important dimension which should be optimized is the distance H between the lower surface of wafer **3** and the top of cup lip **23**. If H is too low, laminar flow apparently results, and there is relatively little offsetting of the "edge effect", resulting in relatively higher bumps near the edge. As H is increased, turbulent flow apparently results, perhaps due to the capillary attraction of the bottom surface of wafer **3** near the edge, and there is increased offsetting of the "edge effect", resulting in edge bumps which are nearly identical in height to bumps elsewhere across the wafer diameter (refer to FIG. **10**).

Flow rate through the plating cup **20** was found not to be a critical parameter. In a preferred embodiment, a flow rate of 4 to 5 liters/minute was employed.

The invention described herein was used successfully to plate bumps comprising an initial layer of silver and a subsequent layer of tin, resulting in metallization bumps substantially as depicted in FIG. **3C**.

FIG. **9** is a graph illustrating the variation of bump height across a silicon wafer electroplated according to the method of the present invention. To produce the results illustrated in FIG. **9**, the height H of wafer **3** above the lip **23** of cup **20** was set at 2.25 millimeters. This produced a bump height variation across the wafer ranging from a high of 43 microns to a low of 35 microns (i.e. with a process variation of approximately 8 microns), which is well within a desired specification width of 20 microns.

FIG. **10** is another graph illustrating the variation of bump height across a silicon wafer electroplated according to the method of the present invention. By raising the height H of wafer **3** above the lip **23** of cup **20** to 2.45 millimeters, the bump height variation across the wafer ranged from a high of 40 microns to a low of 36 microns (i.e. with a process variation of approximately 4 microns). This is a substantial improvement over the process variation of 30 microns produced by the known tank electroplating method.

Description of Alternative Embodiment

FIG. **11** shows an alternative embodiment of apparatus for plating metallization bumps of substantially uniform height onto predetermined terminal areas of a silicon wafer, according to the present invention.

The apparatus illustrated in FIG. **11** differs from that shown in FIG. **7** only in that the distance S between the outer edge of wafer **3** and the inner surface of cup **20** has been increased through the use of an annular ring **100** suitably secured within the lip portion **23** of cup **20**. This is shown merely as one example of how the distance S may be altered.

It will be apparent to those skilled in the art that the disclosed invention may be modified in numerous ways and may assume many embodiments other than the preferred form specifically set out and described above.

For example, the present invention can be extended to electroplating of ceramic substrates. It may also be extended to electroplating metals other than those mentioned herein. The plating cup may take the form of a pipe or other suitable geometric shape.

Accordingly, it is intended by the appended claims to cover all modifications of the invention which fall within the true spirit and scope of the invention.

What is claimed is:

1. A method of forming metallized bumps on predetermined terminal areas of a planar substrate, said bumps being of substantially uniform height across said substrate, wherein said method comprises:

(a) providing a planar substrate having thereon a multiplicity of terminal areas;

(b) applying an electrical potential having a first electrical polarity to said terminal areas;

(c) applying an electrical potential having a second electrical polarity to an electrical terminal immersed in a container of an electroplating solution;

(d) exposing said substrate to said electroplating solution to permit the growth of said metallization bumps on said terminal areas;

(e) controlling the growth of said metallization bumps in a predetermined region of said substrate by altering the metallic ion concentration of said electroplating solution in said predetermined region;

(f) providing said container with an opening whose shape approximates that of said substrate;

(g) positioning said substrate proximate to said container opening;

(h) providing an inlet within said container for pumping said solution into said container, said solution exiting said container through said opening;

wherein said metallic ion concentration of said electroplating solution is changed by:

(i) in step (f) altering the size of said opening;

(j) in step (g) altering the distance of said substrate from said container opening; and

(k) in step (h) altering the flow rate of said solution through said opening.

2. The method of according to claim **1**, wherein said metallization bumps comprise metal selected from the group consisting of silver and tin.

* * * * *

EXHIBIT B

AO 440 (Rev. 8/01) Summons in a Civil Action

UNITED STATES DISTRICT COURT

EASTERN District of TEXAS

ON SEMICONDUCTOR CORPORATION

SUMMONS IN A CIVIL CASE

V.

SAMSUNG ELECTRONICS CO., LTD., et al.

CASE NUMBER:

TO: (Name and address of Defendant)

SAMSUNG AUSTIN SEMICONDUCTOR, L.L.C.
12100 Samsung Blvd.
Austin, Texas 78754

Registered Agent: SUNG WHAN LEE
12100 SAMSUNG BLVD.
AUSTIN TEXAS 78754

YOU ARE HEREBY SUMMONED and required to serve on PLAINTIFF'S ATTORNEY (name and address)

Kenneth R. Adamo, Esq.
Hilda C. Galvan, Esq.
JONES DAY
2727 North Harwood Street
Dallas, TX 75201

an answer to the complaint which is served on you with this summons, within 20 days after service of this summons on you, exclusive of the day of service. If you fail to do so, judgment by default will be taken against you for the relief demanded in the complaint. Any answer that you serve on the parties to this action must be filed with the Clerk of this Court within a reasonable period of time after service.

CLERK

DATE

(By) DEPUTY CLERK

AO 440 (Rev. 8/01) Summons in a Civil Action

RETURN OF SERVICE

Service of the Summons and complaint was made by me[1]	DATE
NAME OF SERVER *(PRINT)*	TITLE

Check one box below to indicate appropriate method of service

☐ Served personally upon the defendant. Place where _____

☐ Left copies thereof at the defendant's dwelling house or usual place of abode with a person of suitable age and discretion then residing therein.

Name of person with whom the summons and complaint were _____

☐ Returned _____

☐ Other (specify): _____

STATEMENT OF SERVICE FEES

TRAVEL	SERVICES	TOTAL

DECLARATION OF SERVER

I declare under penalty of perjury under the laws of the United States of America that the foregoing information contained in the Return of Service and Statement of Service Fees is true and correct.

Executed on _____ _____
Date *Signature of Server*

_____
Address of Server

(1) As to who may serve a summons see Rule 4 of the Federal Rules of Civil Procedure.

UNITED STATES DISTRICT COURT

EASTERN District of TEXAS

ON SEMICONDUCTOR CORPORATION

SUMMONS IN A CIVIL CASE

V.

SAMSUNG ELECTRONICS CO., LTD., et al.

CASE NUMBER:

TO: (Name and address of Defendant)

SAMSUNG ELECTRONICS AMERICA, INC.
105 Challenger Road
Ridgefield Park, New Jersey 07660

Registered Agent: CT Corporation
818 W 7TH ST
LOS ANGELES, CA 90017

YOU ARE HEREBY SUMMONED and required to serve on PLAINTIFF'S ATTORNEY (name and address)

Kenneth R. Adamo, Esq.
Hilda C. Galvan, Esq.
JONES DAY
2727 North Harwood Street
Dallas, TX 75201

an answer to the complaint which is served on you with this summons, within 20 days after service of this summons on you, exclusive of the day of service. If you fail to do so, judgment by default will be taken against you for the relief demanded in the complaint. Any answer that you serve on the parties to this action must be filed with the Clerk of this Court within a reasonable period of time after service.

CLERK

DATE

(By) DEPUTY CLERK

AO 440 (Rev. 8/01) Summons in a Civil Action

RETURN OF SERVICE

Service of the Summons and complaint was made by me[1]	DATE
NAME OF SERVER *(PRINT)*	TITLE

Check one box below to indicate appropriate method of service

☐ Served personally upon the defendant. Place where _____

_____

☐ Left copies thereof at the defendant's dwelling house or usual place of abode with a person of suitable age and discretion then residing therein.

Name of person with whom the summons and complaint were _____

☐ Returned _____

_____

_____

☐ Other (specify): _____

_____

_____

STATEMENT OF SERVICE FEES

TRAVEL	SERVICES	TOTAL

DECLARATION OF SERVER

I declare under penalty of perjury under the laws of the United States of America that the foregoing information contained in the Return of Service and Statement of Service Fees is true and correct.

Executed on _____ _____

Date *Signature of Server*

_____

Address of Server

(1) As to who may serve a summons see Rule 4 of the Federal Rules of Civil Procedure.

UNITED STATES DISTRICT COURT

EASTERN District of TEXAS

ON SEMICONDUCTOR CORPORATION

SUMMONS IN A CIVIL CASE

V.

SAMSUNG ELECTRONICS CO., LTD., et al.

CASE NUMBER:

TO: (Name and address of Defendant)

SAMSUNG SEMICONDUCTOR, INC.
3655 North First Street
San Jose, CA 95134

Registered Agent: NATIONAL REGISTERED AGENTS, INC.
3533 FAIRVIEW INDUSTRIAL DR SE
SALEM, OR 97302

YOU ARE HEREBY SUMMONED and required to serve on PLAINTIFF'S ATTORNEY (name and address)

Kenneth R. Adamo, Esq.
Hilda C. Galvan, Esq.
JONES DAY
2727 North Harwood Street
Dallas, TX 75201

an answer to the complaint which is served on you with this summons, within 20 days after service of this summons on you, exclusive of the day of service. If you fail to do so, judgment by default will be taken against you for the relief demanded in the complaint. Any answer that you serve on the parties to this action must be filed with the Clerk of this Court within a reasonable period of time after service.

CLERK

DATE

(By) DEPUTY CLERK

AO 440 (Rev. 8/01) Summons in a Civil Action

RETURN OF SERVICE

Service of the Summons and complaint was made by me[1]	DATE
NAME OF SERVER *(PRINT)*	TITLE

Check one box below to indicate appropriate method of service

☐ Served personally upon the defendant. Place where _____

_____

☐ Left copies thereof at the defendant's dwelling house or usual place of abode with a person of suitable age and discretion then residing therein.

Name of person with whom the summons and complaint were _____

☐ Returned _____

_____

_____

☐ Other (specify): _____

_____

_____

STATEMENT OF SERVICE FEES

TRAVEL	SERVICES	TOTAL

DECLARATION OF SERVER

I declare under penalty of perjury under the laws of the United States of America that the foregoing information contained in the Return of Service and Statement of Service Fees is true and correct.

Executed on _____ _____

Date *Signature of Server*

_____

Address of Server

(1) As to who may serve a summons see Rule 4 of the Federal Rules of Civil Procedure.

UNITED STATES DISTRICT COURT

EASTERN District of TEXAS

ON SEMICONDUCTOR CORPORATION

SUMMONS IN A CIVIL CASE

V.

SAMSUNG ELECTRONICS CO., LTD., et al.

CASE NUMBER:

TO: (Name and address of Defendant)

SAMSUNG TELECOMMUNICATIONS AMERICA GENERAL, L.L.C.
1301 East Lookout Drive
Richardson, Texas 75082

Registered Agent: PAMELA DAY
1301 East Lookout Drive
Richardson, Texas 75082

YOU ARE HEREBY SUMMONED and required to serve on PLAINTIFF'S ATTORNEY (name and address)

Kenneth R. Adamo, Esq.
Hilda C. Galvan, Esq.
JONES DAY
2727 North Harwood Street
Dallas, TX 75201

an answer to the complaint which is served on you with this summons, within 20 days after service of this summons on you, exclusive of the day of service. If you fail to do so, judgment by default will be taken against you for the relief demanded in the complaint. Any answer that you serve on the parties to this action must be filed with the Clerk of this Court within a reasonable period of time after service.

CLERK

DATE

(By) DEPUTY CLERK

✎ AO 440 (Rev. 8/01) Summons in a Civil Action

RETURN OF SERVICE

Service of the Summons and complaint was made by me[1]	DATE
NAME OF SERVER *(PRINT)*	TITLE

Check one box below to indicate appropriate method of service

☐ Served personally upon the defendant. Place where _____

_____

☐ Left copies thereof at the defendant's dwelling house or usual place of abode with a person of suitable age and discretion then residing therein.

Name of person with whom the summons and complaint were _____

☐ Returned _____

_____

_____

☐ Other (specify): _____

_____

_____

STATEMENT OF SERVICE FEES

TRAVEL	SERVICES	TOTAL

DECLARATION OF SERVER

I declare under penalty of perjury under the laws of the United States of America that the foregoing information contained in the Return of Service and Statement of Service Fees is true and correct.

Executed on _____ _____

Date *Signature of Server*

_____

Address of Server

(1) As to who may serve a summons see Rule 4 of the Federal Rules of Civil Procedure.